SPECIFICATIONS FOR DESIGN, DEVELOPMENT AND FABRICATION OF BURN-IN JIG TO SCREEN 44PIN JLEAD RCNW1451TP

JULY 2019

U R RAO SATELLITE CENTRE
INDIAN SPACE RESEARCH ORGANISATION
BANGALORE
SPECIFICATIONS FOR DESIGN, DEVELOPMENT AND FABRICATION OF BURN-IN JIG TO SCREEN 44PIN JLEAD RCNW1451TP

1.0 GENERAL
Burn-in Jig consists of Burn-in unit, polyamide burn-in board and a harness to connect the burn-in board to burn-in unit. Realization of burn-in unit and burn-in board involves schematic entry, PCB layout design, filming, PCB fabrication, wiring of PCB, wiring of interface harness, integrated testing, housing of the electronic hardware in an appropriate mechanical package with aesthetic addition viz. screen printing, painting, etc. and supply of detailed operational and inter connection document.

2.0 Description of 44PIN JLEAD RCNW1451TP (See fig. 1)
1451TP is a RC network for Thermistor processing and monitoring at 5V. Single RC network contains 10 kΩ & 22 kΩ resistor with 1kpf capacitor. The 44 pin J lead RCNW 1451TP consists of 16 RC networks. 5V bias supply voltage is provided for this RCNW. Supply & ground pins are common to all the sixteen processing networks.

3.0 Mechanical packaging details of 44PIN JLEAD RCNW1451TP (See Fig. 2)
No. of pins : 44 pin
Substrate Size : 0.65” x 0.65”
Overall Package size : 0.67” x 0.67” (No encapsulation)

4.0 Work description:
The work involves development and fabrication of Burn-in unit, polyamide burn-in boards and connecting harnesses with proper document generation.

4.1.0 Description of RCNW Burn-in Unit
This unit should generate the required signals for the RCNWs. Burn-in configuration is provided in section 6.0. Also, provision shall be made for monitoring Vcc, ground, input signals, RCNW outputs and total current drawn by the RCNWs.
Figure 1. Internal Circuit Diagram of 44PIN JLEAD RCNW

SCHEMATIC OF RC NETWORK 1451TP

R1 - R16 = 10 KOHMS, ±2%, 20mW
R17 - R32 = 22 KOHMS, ±2%, 20mW
C1 - C16 = CDR01/CDR31 1KPF, ±10%, 100V

PIN NO. 4 & 30 = VCC
PIN NO. 12 & 21 = GND
PIN NO. 3, 11, 22, 25, 33, 34, 35 & 44 = NC

ISAC  DATE  SIGN  01/08/2014  01  00  SCHEMATIC OF 1451TP RC NETWORK
DRAWN
CHECKED
QUALITY

ISRO SATELLITE CENTRE, BANGALORE 560017
Figure 2. Mechanical packaging details of 44PIN JLEAD RCNW 1451TP
4.1.1 Burn-in Unit consists of:

a) Signal generation cards.
b) Interface connectors to burn-in PCB.
c) Monitoring sockets for RCNW o/ps.
d) Monitoring Sockets for Vcc
e) RCNW current monitoring terminals.
f) Monitoring of input signals.
g) Supply I/P terminals and monitoring terminals.
h) Power ON switch for +5V & +50V Supply.

4.1.2 Burn-in Card:

The burn-in card should be designed so as to accommodate 12 RCNWs in a single card. YAMAICHI sockets (Part No: IC51-0444-400) should be used to mount RCNWs on cards. These socket’s lids are to be milled to place the RCNW without damage. Four burn-in boards shall be used for a burn-in Jig. In total burn-in can be carried out on 48 nos of 44 pin J Lead RCNWs 1451TP with single burn-in jig.

4.2 Document

A detailed document both soft copy and hard copy to be supplied as per the list given below:

- Schematic diagrams
- PCB film
- Component marking print
- PTH marking print
- Net list
- I/O details of each connector
- Box wiring details

4.3 General Specifications for PCB Design (Two Layers only)

Following procedures are to be followed and approval from the Subsystem to be obtained for the final schematic diagrams before proceeding to next stage. Inspection by the vendor’s internal QA to be carried out at various stages and report for the same in the format prescribed in the PMPD document (Doc No. INT: PMPD/SPES/HMC/GEN/13/REV-8) to be submitted along with the final unit.

4.3.1 General guidelines for Layout Design:

No. Of layers: Two

Following track widths are to be provided:

<table>
<thead>
<tr>
<th>Sl.No.</th>
<th>Signal Description</th>
<th>Track Width</th>
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<tbody>
<tr>
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</tr>
<tr>
<td>4.</td>
<td>Board edge to electrical components spacing</td>
<td>200 MIL Min.</td>
</tr>
</tbody>
</table>

4.3.2 Filming

Filming has to be done with standard material of 7 MIL thick polymer based material.
4.3.3 PCB Fabrication

a) PCB has to be fabricated using Polyamide board base material for Burn-in PCB and glass epoxy for PCBs in Burn-in test unit with thickness 1.6mm and solder masks with conformal coating and screen printing of component names to be done wherever required.

b) Bare Board Test (BBT) report to be furnished before wiring components on PCB.

4.3.4 PCB Wiring

As these PCBs are subjected to thermal cycling, the components are to be soldered using good quality solder; the part no. as mentioned below shall be used.

Spec./Part No.: 5 core, SN63PB37, 21 gauge RMA flux.

Additional external Flux shall not be used for wiring Burn-in PCBs.

All layer changing VIAs (PTHs) on the PCB to be filled with solder.

5.0 RCNW 1451 TP Circuit Diagram: Is given in Fig:1.

6.0 Burn-in configuration of 1451TP

Connection Details:

a) Short Vcc(pin nos: 4 & 30) of all RCNWs and mark it as High.

b) Short all output ((pin nos: 1, 6, 7, 10, 13, 16, 17, 20, 23, 27, 28, 32, 36, 39, 40 & 43) pins and Ground pins (pin no: 12 & 21) of all RCNWs and mark it as Low.

c) Leave all input pins (pin nos: 2, 5, 8, 9, 14, 15, 18, 19, 24, 26, 29, 31, 37, 38, 41 & 42) open.

d) Connect a 100µsec pulse (with 25% duty cycle) of amplitude 50V between High and Low points.

Test Duration:

96 hours at 70°C with a duty cycle of 1 ½ hours ON and ½ hour OFF.

6.1 Burn-in Card:

A) Specifications for Burn-in Card Design

No. of 44pin RCNWs: 12 per PCB (Spacing for mounting. YAMAICHI sockets to be provided)

PCB size: Maximum 12” x 12”
Input / Output : Amphenol connectors part nos given in SOW document
Thickness of PCB : 1.6mm

B) Layout Design:
No. of layers : Two
Following track widths are to be provided:

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C) Mechanical drawing of YAMAICHI(IC51-0444-400) Socket: Is provided at the end of document 6.

6.2 Output monitoring:

RCNW I/P & O/P Monitoring
Input signals & 192 outputs from 12 RCNWs (16 outputs/RCNW) for one board to be monitored during course of testing. 4 connector sockets for one board and hence total 16 connectors for 4 boards are required to be provided. Hence, for output monitoring 50 pin connector sockets shall be provided on the top panel of the test unit.

RCNW Current Monitoring
Provision shall be made to connect an external Ammeter to monitor the total current taken by each burn-in PCB (6 RCNWs). Current drawn by the burn-in unit should not be included in any of these RCNW current monitoring.

Supply Input & Monitoring
DC voltage of +5V & +50V is fed from external Power Supply. Hence suitable lamp post terminals shall be provided for the same in the front panel.

Monitoring points for supplies and Gnd to be provided on the top panel.

6.3 Harness and Connector Details:
The part nos of connectors and specifications for wires provided in SOW are to be followed.

7.0 Deliverables By Vendor

Burn-in PCBs - As per indent
Burn-in test unit - As per indent
All relevant documents -
Approved PCB L/Os all types
Approved gerber files: Layout for both sides, Component marking, PTH marking, drill details prints
Approved PCB film
Unit interconnection details and Operation manual
Hard copy and soft copy in CD for the above details shall be provided.

Interface test harness of length 2.2 meter – Qty. as per indent
Burn-in PCB photo film, layout, hard & soft copy for each of the PCB designed, developed or issued.

8.0 Documentation:
As mentioned in the statement of work a detailed document both soft copy and hard copy to be supplied as per the list given below:

- Schematic diagrams
- PCB film details
- Gerber files for all layers
- Component marking print
- PTH marking print
- Net list
- I/O details of each connector
- Box wiring details

9.0 ACCEPTANCE CRITERIA
1. Vendor should obtain acceptance from the Subsystem for the Circuit schematic diagram.
2. Bare PCB to be inspected by vendor's QA before mounting/ wiring of components. Initial electrical tests to be carried out at vendor's place only.
3. Only one unit shall be fabricated first and after obtaining the acceptance from subsystem and HQCS for the same, subsequent units shall be fabricated.
4. The unit as a whole along with burn-in PCB, test unit and interface harness, will be accepted after performance test in detail demonstrated at vendor's place and certified by the indenting subsystem and HQCS.
5. Vendor shall be ready to conduct the detailed demonstration at URSC if instructions are given for the same.
6. Vendor should strictly adhere to the delivery conditions as mentioned in P.O.

REJECTION CRITERIA
The layout design or PCB or the unit as a whole will be rejected if it does not meet the required specifications as mentioned before. In case of any deviations in layout making, filming, PCB fabrication, wiring, testing the material, damages to the material supplied by URSC (if any) etc, the card or unit to be replaced free of cost by the vendor and replacement of unit/card should meet the specifications.

SECRECY
Vendor should not disclose or give details of the specifications in any form to anyone without the explicit permission from URSC. To this extent vendor has to execute a non-disclosure/secrecy agreement.

10.0 Warranty
All the items supplied to be warranted for a period of one year form the date of acceptance and any defective parts systems are to be replaced free of cost during warranty period.

Note: For the realization of the above work the guideline documentis:

STATEMENT OF WORK TO FABRICATE FUNCTIONAL TEST/BURN-IN TEST JIGS FOR TESTING HYBRID MICRO CIRCUITS
Unless specified in this indent guideline mentioned in the above document are binding for the fabrication work.

DOC NO. 2: 1451TP/ JULY 19/FTJ

SPECIFICATIONS FOR DESIGN, DEVELOPMENT AND FABRICATION OF FUNCTIONAL TEST JIG TO TEST/SCREEN 44PIN JLEAD RCNW1451TP

JULY 2019

U R RAO SATELLITE CENTRE
INDIAN SPACE RESEARCH ORGANISATION
BANGALORE
1.0 GENERAL

Realization of functional test jig involves schematic entry, PCB layout design, filming, PCB fabrication, wiring of PCB, integrated testing, housing of the electronic hardware in an appropriate mechanical package with aesthetic addition viz. screen printing, painting, etc, box wiring and supply of detailed operational and interconnection document.

2.0 Description of 44PIN JLEAD RCNW1451TP (See fig.1)

1451TP is a RC network for Thermistor processing and monitoring at 5V. Single RC network contains 10 kΩ & 22 kΩ resistor with 1kpf capacitor. The 44 pin J lead RCNW 1451TP consists of 16 RC networks. 5V bias supply voltage is provided for this RCNW. Supply & ground pins are common to all the sixteen processing networks.

3.0 Mechanical packaging details of 44PIN JLEAD RCNW1451TP (See Fig. 2)

<table>
<thead>
<tr>
<th>No. of pins</th>
<th>44 pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>Substrate Size</td>
<td>0.65” x 0.65”</td>
</tr>
<tr>
<td>Overall Package size</td>
<td>0.67” x 0.67” (No encapsulation)</td>
</tr>
</tbody>
</table>

4.0 Work description:

The work involves development and fabrication of functional test jig with proper document generation.

4.1 Description of J lead RCNW Functional Test Jig

This unit should provide interface for the necessary signals for the RCNW under test. Necessary input simulation signals are to be generated for simulating the inputs. Provision must be made to provide external signal. It also should have provision to connect or disconnect the input signal to Vcc. Therefore, it is required to make int/ext switch for feeding internal/external stimuli. This unit should have front panel monitoring for the input simulation signal, RCNW inputs, outputs, Vcc and ground.
Figure1. Internal Circuit Diagram of 44PIN JLEAD RCNW1451TP
Figure 2. Mechanical packaging details of 44PIN JLEAD RCNW1451TP: given in Document1.
Layout of 1451TP
4.1.1 Functional Test Jig consists of:

i) Signal generation card.

j) YAMAICHI socket (part no: IC51-0444-400) card for placing the J Lead 44 pin RCNW during its functional test.

k) Provision for RCNW I/P, O/P monitoring.

l) Monitoring socket for simulation signal input.

m) Supply and gnd.

n) Power ON switch for +5 V Supply.

4.2 Document

A detailed document both soft copy and hard copy to be supplied as per the list given below:

- Schematic diagrams
- PCB film
- Component marking print
- PTH marking print
- Net list
- Front & back panel diagram of the box.
- Box wiring details
- How to use the jig and any other relevant information.

4.3.0 General Specifications for PCB Design (Two Layers only)

Following procedures are to be followed and approval from the Subsystem to be obtained for the final schematics diagram before proceeding to next stage. Inspection by the vendor's internal QA to be carried out at various stages and report for the same in the format prescribed in the PMPD document (Doc No. INT: PMPD/SPES/HMC/GEN/13/REV-8) to be submitted along with the final unit.

4.4.1 General guidelines for Layout Design:

No. Of layers: Two

Following track widths are to be provided:

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</table>
4.4.2 Filming
Filming has to be done with standard material of 7 MIL thick polymer based material. Contact film is not acceptable

4.4.3 PCB Fabrication
a) PCB has to be fabricated using glass epoxy with thickness 1.6mm and solder masks with conformal coating and screen printing of component names to be done wherever required.

b) Bare Board Test (BBT) report to be furnished before wiring components on PCB.

4.4.4 PCB Wiring
The components shall be soldered using good quality solder; the part number mentioned below shall be used.

Spec./Part No. : 5 core, SN63PB37, 21 gauge RMA flux.
All layer changing VIAs (PTHs) on the PCB to be filled with solder.

5.0 RCNW Circuit Diagram: Given in Fig1.

6.0 Electrical Test Specifications & Electrical Test Procedure:

- Measure the Resistance between Vcc (pin nos: 4 & 30) and I/P (pin nos: 2, 5, 8, 9, 14, 15, 18, 19, 24, 26, 29, 31, 37, 38, 41 & 42) pins.
  Typical Value = 10 kΩ with a tolerance of 2%. So the expected value is 9.8 kΩ to 10.2 kΩ.

- Measure the Resistance between I/P (pin nos: 2, 5, 8, 9, 14, 15, 18, 19, 24, 26, 29, 31, 37, 38, 41 & 42) and O/P (pin nos: 1, 6, 7, 10, 13, 16, 17, 20, 23, 27, 28, 32, 36, 39, 40 & 43) pins.
  Typical Value = 22 kΩ with a tolerance of 2%. The expected value is 21.56 kΩ to 22.44 kΩ.

- Measure the capacitance between O/P (pin nos: 1, 6, 7, 10, 13, 16, 17, 20, 23, 27, 28, 32, 36, 39, 40 & 43) pins and Ground pins (pin no: 12 & 21).
  Typical Value = 1kpf with a tolerance of 10%. The expected value is 0.9kpf to 1.1kpf.

- Give a pulse train of 2.5 khz, 100 μsec pulse width, 5V to Vcc (pin nos: 4 & 30) and check the O/Ps (pin nos: 1, 6, 7, 10, 13, 16, 17, 20, 23, 27, 28, 32, 36, 39, 40 & 43) pins.
  The settling time expected is ≈ 50-μsec-±20% i.e. 40 to 60 μsec.

7.0 Block Diagram of Functional Test Jig:
Block diagram of functional test jig and the test set up is given in Fig:4
8.0 RCNW O/P Monitoring

RCNW outputs are to be monitored during testing. Hence for this purpose suitable output monitoring sockets are to be provided on the front panel of the unit.

9.0 Monitoring of Input Signal

A suitable socket shall be provided in the front panel to monitor the input signal.

10.0 Supply Input & Monitoring

DC voltage of +5V is fed from external Power Supply. Hence suitable lamp post terminals shall be provided for the same.

Monitoring point, preferably terminal post shall be provided on the front panel for the power supply monitoring for +5V.

11.0 Interconnection Details:

The signal generation card and Yamaichi socket cards are to be interconnected and the connection details shall be incorporated in document.
The front panel selections and monitoring are to be wired from the signal generation card by adopting appropriate box wiring procedures.

12.0 Component List
Vendor shall procure all the materials for the realization of the test unit, including Yamaichi socket and MIL grade components.

Yamaichi socket shall be milled to accommodate the RCNW with ease and without disturbing the encapsulation of RCNW.

13.0 Deliverables by vendor
- Functional test unit
- All relevant documents
- Approved PCB L/Os all types
- Approved spool files, component marking, PTH marking, drill detail prints
- Approved PCB film
- Box interconnection details
- Operation manual
Hard copy in duplicate and soft copy in CD for the above details shall be provided.

14.0 Documentation:
As mentioned in the statement of work a detailed document both soft copy and hard copy shall be supplied as per the list given below:
- Schematic diagrams
- PCB film details
- Component marking print
- PTH marking print
- Net list
- I/O details of each connector
- Box wiring details

15.0 ACCEPTANCE CRITERIA
1. Vendor should obtain acceptance from the Subsystem for the Circuit schematic diagram.
2. Bare PCB to be inspected by vendor's QA before mounting/wiring of components. Initial electrical tests to be carried out at vendor's place only.
3. Only one unit shall be fabricated first and after obtaining the acceptance from subsystem and SRG for the same, subsequent units shall be fabricated.
4. The unit will be accepted after performance test in detail demonstrated at vendor's place and certified by the indenting subsystem and SRG.
5. Vendor shall be ready to conduct the detailed demonstration at ISAC if instructions are given for the same.
6. Vendor should strictly adhere to the delivery conditions as mentioned in P.O.
16.1 REJECTION CRITERIA
The layout design or PCB or the unit as a whole will be rejected if it does not meet the required specifications as mentioned before. In case of any deviations in layout making, filming, PCB fabrication, wiring, testing the material, damages to the material supplied by ISAC (if any) etc, the card or unit to be replaced free of cost by the vendor and replacement of unit/card should meet the specifications.

16.2 SECRECY
Vendor should not disclose or give details of the specifications in any form to any one without the explicit permission from ISAC. To this extent vendor has to execute a non-disclosure/secrecy agreement.

17.0 Warranty
All the items supplied to be warranted for a period of one year from the date of acceptance and any defective parts systems are to be replaced free of cost during warranty period.

Note: For the realization of the above work the guideline document is:

STATEMENT OF WORK TO FABRICATE FUNCTIONAL TEST/BURN-IN TEST JIGS FOR TESTING HYBRID MICRO CIRCUITS

Unless specified in this indent guideline mentioned in the above documents are binding for the fabrication work.
SPECIFICATIONS FOR DESIGN, DEVELOPMENT AND FABRICATION OF BURN-IN JIG TO SCREEN 44PIN JLEAD RCNW1461LF

JULY 2019

U R RAO SATELLITE CENTRE
INDIAN SPACE RESEARCH ORGANISATION
BANGALORE
SPECIFICATIONS FOR DESIGN, DEVELOPMENT AND FABRICATION OF BURN-IN JIG TO SCREEN 44PIN JLEAD RCNW1461LF

1.0 GENERAL
Burn-in Jig consists of Burn-in unit, polyamide burn-in board and a harness to connect the burn-in board to burn-in unit. Realization of burn-in unit and burn-in board involves schematic entry, PCB layout design, filming, PCB fabrication, wiring of PCB, wiring of interface harness, integrated testing, housing of the electronic hardware in an appropriate mechanical package with aesthetic addition viz. screen printing, painting, etc. and supply of detailed operational and interconnection document.

2.0 Description of 44PIN JLEAD RCNW1461LF (See fig. 1)
1461LF is a RC filter network for processing analog channels without pull-down resistor. The filter time constant is 103µs. Single RC network contains 22 kΩ resistor with 4.7kpf capacitor. The 44 pin J lead RCNW 1461LF consists of 16 RC networks. All these networks have common ground pins.

3.0 Mechanical packaging details of 44PIN JLEAD RCNW1461LF (See Fig. 2)
No. of pins : 44 pin
Substrate Size : 0.65” x 0.65”
Overall Package size : 0.67” x 0.67” without encapsulation.

4.0 Work description:
The work involves development and fabrication of Burn-in unit, polyamide burn-in boards and connecting harnesses with proper document generation.

4.1.0 Description of RCNW Burn-in Unit
This unit should generate the required signals for the RCNWs. This unit should have a load resistor card to load outputs of the RCNWs. Burn-in configuration is provided in section 6.0. Also, provision shall be made for monitoring supplies, ground, inputs and total current drawn by the RCNWs.
Figure 1. Internal Circuit Diagram of 44PIN JLEAD RCNW 1461LF

Schematic of RC Network 1461LF

R1 - R16 = 22 KOhms, ±10%, 20mW
C1 - C16 = CDRO1/CDRO3 4.7KPF, ±10%, 100V
PIN NO. 12 & 21 = GND
PIN NO. 3, 4, 11, 22, 25, 30, 33, 34, 35 & 44 = NC

ISAC DATE SIGN
DRAWN
CHECKED
QUALITY

13/05/2015

1461LF RC NETWORK

ISRO SATELLITE CENTRE, BANGALORE 560017
MECHANICAL DRAWING OF 44 PIN CQFJ RC NETWORKS

PART NUMBERS:
1. 1451TP
2. 1461LF
3. 1471LF

NOTE:
1. ALL DIMENSIONS ARE IN:INCHES
2. GENERAL TOL. +/-.001
   UNLESS OTHERWISE SPECIFIED

PIN DETAILS:
SURFACE MOUNT J-LEAD WITH 0.050" PITCH
MATERIAL: BERYLLIUM COPPER
(POST PLATED Sn60/Pb40)
MAKE: NAS INTERPLEX INC. USA
P/N.: CC21AA-D22V-0KFD
SOLDER TYPE: Sn63/Pb37
PIN STAND OFF HEIGHT: 0.145"
4.1.1 Burn-in Unit consists of:

- Signal generation card.
- Interface connectors to burn-in PCB.
- Output loading resistor card.
- Monitoring sockets for i/p/s.
- RCNW current monitoring terminals.
- Monitoring of input signals.
- Supply I/P terminals and monitoring terminals.
- Power ON switch for +5V & +50V Supply.

4.1.3 Burn-in Card:

The burn-in card should be designed so as to accommodate 12RCNWs in a single card. **YAMAICHI** sockets (Part No: **IC51-0444-400**) should be used to mount RCNWs on cards. **These socket's lids are to be milled to place the RCNW without damage.** Four burn-in boards shall be used for a burn-in jig. Therefore, burn-in can be carried out on 48 nos of 44 pin J Lead RCNWs 1461LF with single burn-in jig.

4.2 Document

A detailed document both soft copy and hard copy to be supplied as per the list given below:

1. Schematic diagrams
2. PCB film
3. Component marking print
4. PTH marking print
5. Net list
6. I/O details of each connector
7. Box wiring details

4.3 General Specifications for PCB Design (Two Layers only)

Following procedures are to be followed and **approval from the Subsystem** to be obtained for the final schematics diagram before proceeding to next stage. Inspection by the vendor's internal QA to be carried out at various stages and report for the same in the format prescribed in the PMPD document (Doc No. INT: PMPD/SPES/HMC/GEN/13/REV-8) to be submitted along with the final unit.

4.3.1 General guidelines for Layout Design:

| No. of layers | Two |

Following track widths are to be provided:

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</table>
4.3.2 Filming

Filming has to be done with standard material of 7 MIL thick polymer based material. Contact film is not acceptable.

4.3.3 PCB Fabrication

c) PCB has to be fabricated using Polyamide board base material for Burn-in PCB and glass epoxy for PCBs in Burn-in test unit with thickness 1.6mm and solder masks with conformal coating and screen printing of component names to be done wherever required.

d) Bare Board Test (BBT) report to be furnished before wiring components on PCB.

4.3.4 PCB Wiring

As these PCBs are subjected to thermal cycling, the components are to be soldered using good quality solder; the part no. as mentioned below shall be used.

Spec./Part No.: 5 core, SN63PB37, 21 gauge RMA flux.

Additional external Flux shall not be used for wiring Burn-in PCBs.

All layer changing VIAs (PTHs) on the PCB to be filled with solder.

5.0 RCNW 1461 LF Circuit Diagram: Shown in Fig:1

6.0 Burn-in configuration of 1461LF

Connection Details:

a) Short all Input (pin nos: 1, 6, 7, 10, 13, 16, 17, 20, 23, 27, 28, 32, 36, 39, 40 & 43) pins and Ground pins (pin no: 12 & 21) of all RCNWs and mark it as Low.

b) Short all output pins (pin nos: 2, 5, 8, 9, 14, 15, 18, 19, 24, 26, 29, 31, 37, 38, 41 & 42) of each RCNW, to this connect a 2.7kΩ resistor one end; mark other end of 2.7 kΩ resistor as High.

c) Connect a 1 msec pulse (frequency-1kHz with 50% duty cycle) of amplitude 50V between High and Low points.

Test Duration:

96 hours at 70°C with a duty cycle of 1 ½ hours ON and ½ hour OFF.

6.1 Burn-in Card:

A) Specifications for Burn-in Card Design

No. of 44pin RCNWs: 12 per PCB (Spacing for mounting. 
YAMAICHI sockets to be provided)

PCB size: maximum 12" x 12"

Input / Output: Amphenol connectors part nos given in SOW document

Thickness of PCB: 1.6mm

B) Layout Design:
No. of layers: Two
Following track widths are to be provided:

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</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Supply lines</td>
<td>40 MIL min.</td>
</tr>
<tr>
<td>2.</td>
<td>Control signal lines</td>
<td>20 MIL min.</td>
</tr>
<tr>
<td>3.</td>
<td>Spacing between tracks, pads, vias</td>
<td>20 MIL min.</td>
</tr>
<tr>
<td>4.</td>
<td>Board edge to electrical components spacing</td>
<td>200 L min.</td>
</tr>
</tbody>
</table>

C) Mechanical drawing of YAMAICHI(IC51-0444-400) Socket: Is provided at the end of document 6.

6.2 Output monitoring:

RCNW I/P & O/P Monitoring
Input signals to RCNWs of 4 boards are to be monitored during course of testing. For this purpose, suitable monitoring points to be provided on the top panel.

RCNW Current Monitoring
Provision shall be made to connect one external Ammeters to monitor the current taken by individual burn-in PCB (12RCNWs). Hence provision shall be made to connect 4 current meters for 4 boards. Current drawn by the burn-in unit should not be included in any of these RCNW current monitoring.

Supply Input & Monitoring
DC voltage of +5V & +50V is fed from external Power Supply. Hence suitable lamp post terminals shall be provided for the same in the front panel.
Monitoring points for supplies and Gnd to be provided on the top panel.

6.3 Harness and Connector Details:
The part nos of connectors and specifications for wires provided in SOW are to be followed.

7.0 Deliverables by Vendor

Burn-in PCBs - As per indent
Burn-in test unit - As per indent
All relevant documents -
Approved PCB L/Os all types
Approved spool files, component marking, PTH marking, drill details prints
Approved PCB film
Unit interconnection details and Operation manual
Hard copy in duplicate and soft copy in CD for the above details shall be provided.
Interface test harness of length 2.2 meter – Qty. as per indent
Burn-in PCB photo film, layout, hard & soft copy for each of the PCB designed, developed or issued.

8.0 Documentation: As mentioned in the statement of work a detailed document both soft copy and hard copy to be supplied as per the list given below:
1. Schematic diagrams
2. PCB film details
3. Gerber files for all layers
4. Component marking print
5. PTH marking print
6. Net list
7. I/O details of each connector
8. Box wiring details

9.0 ACCEPTANCE CRITERIA

1. Vendor should obtain acceptance from the Subsystem for the Circuit schematic diagram.
2. Bare PCB to be inspected by vendor’s QA before mounting/wiring of components. Initial electrical tests to be carried out at vendor’s place only.
3. Only one unit shall be fabricated first and after obtaining the acceptance from subsystem and HQCS for the same, subsequent units shall be fabricated.
4. The unit as a whole along with burn-in PCB, test unit and interface harness, will be accepted after performance test in detail demonstrated at vendor’s place and certified by the indenting subsystem and HQCS.
5. Vendor shall be ready to conduct the detailed demonstration at URSC if instructions are given for the same.
6. Vendor should strictly adhere to the delivery conditions as mentioned in P.O.

10. REJECTION CRITERIA

The layout design or PCB or the unit as a whole will be rejected if it does not meet the required specifications as mentioned before. In case of any deviations in layout making, filming, PCB fabrication, wiring, testing the material, damages to the material supplied by URSC (if any) etc, the card or unit to be replaced free of cost by the vendor and replacement of unit/card should meet the specifications.

11. SECRECY

Vendor should not disclose or give details of the specifications in any form to anyone without the explicit permission from URSC. To this extent vendor has to execute a non-disclosure/secrecy agreement.

12. Warranty

All the items supplied to be warranted for a period of one year from the date of acceptance and any defective parts systems are to be replaced free of cost during warranty period.

Note: For the realization of the above work the guideline document is:

STATEMENT OF WORK TO FABRICATE FUNCTIONAL TEST/BURN-IN TEST JIGS FOR TESTING HYBRID MICRO CIRCUITS

Unless specified in this indent guideline mentioned in the above document are binding for the fabrication work.
SPECIFICATIONS FOR DESIGN, DEVELOPMENT AND FABRICATION OF FUNCTIONAL TEST JIG TO TEST/SCREEN 44PIN JLEAD RCNW1461LF

JULY 2019

U R RAO SATELLITE CENTRE
INDIAN SPACE RESEARCH ORGANISATION
BANGALORE
SPECIFICATIONS FOR DESIGN, DEVELOPMENT AND FABRICATION OF FUNCTIONAL TEST JIG TO TEST/SCREEN 44PIN JLEAD RCNW1461LF

1.0 GENERAL
Realization of functional test jig involves schematic entry, PCB layout design, filming, PCB fabrication, wiring of PCB, integrated testing, housing of the electronic hardware in an appropriate mechanical package with aesthetic addition viz. screen printing, painting, etc., box wiring and supply of detailed operational and interconnection document.

2.0 Description of 44PIN JLEAD RCNW1461LF (See Fig. 1)

1461LF is a RC filter network for processing analog channels without pull-down resistor. The filter time constant is 103\(\mu\)s. Single RC network contains 22 k\(\Omega\) resistor with 4.7kpf capacitor. The 44 pin J lead HMC 1461LF consists of 16 RC networks. All these networks have common ground pins.

3.0 Mechanical packaging details of 44PIN JLEAD RCNW1461LF (See Fig. 2)

<table>
<thead>
<tr>
<th>Details</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>No. of pins</td>
<td>44 pin</td>
</tr>
<tr>
<td>Substrate Size</td>
<td>0.65&quot; x 0.65&quot;</td>
</tr>
<tr>
<td>Overall Package size</td>
<td>0.67&quot; x 0.67&quot;</td>
</tr>
</tbody>
</table>

4.0 Work description:
The work involves development and fabrication of functional test jig with proper document generation.

4.1 Description of J lead RCNW 1461 LF Functional Test Jig
This unit should provide interface for the necessary signals for the RCNW under test. Necessary input simulation signals are to be generated for simulating the inputs. Provision must be made to provide external signal. It also should have provision to connect or disconnect the input signal to input pins. Therefore, it is required to make int/ext switch for feeding internal/external stimuli. This unit should have front panel monitoring for the input simulation signal, RCNW inputs, outputs and ground.
Figure 1. Internal Circuit Diagram of 44PIN JLEAD RCNW1461LF

SCHEMATIC OF RC NETWORK 1461LF

R1 - R16 = 22 KOHMS, ±10%, 20mW
C1 - C16 = CDR01/CDR31 4.7KPF, ±10%, 100V
PIN NO. 12 & 21 = GND
PIN NO. 3, 4, 11, 22, 25, 30, 33, 34, 35 & 44 = NC

ISAC SATELLITE CENTRE, BENGALURU 560017
Figure 2. Mechanical packaging details of 44PIN JLEAD RCNW1461LF: See Document 1.

Layout of 1461LF
4.2.1  Functional Test Jig consists of:

a) Signal generation card.

b) YAMAICHI socket (part no: IC51-0444-400) card for placing the Jlead 44 pin RCNW during its functional test.

c) Provision for RCNW I/P, O/P monitoring.

d) Monitoring socket for simulation signal input.

e) Supply and gnd.

f) Power ON switch for +5 V Supply.

4.3  Document

A detailed document both soft copy and hard copy to be supplied as per the list given below:

- Schematic diagrams
- PCB film
- Gerber files for all layers.
- Component marking print
- PTH marking print
- Net list
- Front & back panel diagram of the box.

4.3.0  General Specifications for PCB Design (Two Layers only)

Following procedures are to be followed and approval from the Subsystem to be obtained for the final schematics diagram before proceeding to next stage. Inspection by the vendor's internal QA to be carried out at various stages and report for the same in the format prescribed in the PMPD document (Doc No. INT: PMPD/SPES/HMC/GEN/13/REV-8) to be submitted along with the final unit.

4.4.5  General guidelines for Layout Design:

No. Of layers: Two

Following track widths are to be provided:

<table>
<thead>
<tr>
<th>Sl.No.</th>
<th>Signal Description</th>
<th>Track Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Supply lines</td>
<td>40 MIL Min.</td>
</tr>
<tr>
<td>2.</td>
<td>Control signal lines</td>
<td>15 MIL Min.</td>
</tr>
<tr>
<td>3.</td>
<td>Spacing between tracks, pads, vias</td>
<td>12 MIL Min.</td>
</tr>
<tr>
<td>4.</td>
<td>Board edge to electrical components spacing</td>
<td>200 MIL Min.</td>
</tr>
</tbody>
</table>

4.4.6  Filming

Filming has to be done with standard material of 7 mil thick polymer based material. Contact film is not acceptable.

4.4.7  PCB Fabrication
c) PCB has to be fabricated using glass epoxy with thickness 1.6mm and solder masks with conformal coating and screen printing of component names to be done wherever required.

d) Bare Board Test (BBT) report to be furnished before wiring components on PCB.

4.4.8 PCB Wiring

The components shall be soldered using good quality solder; the part number mentioned below shall be used.

Spec./Part No.: 5 core, SN63PB37, 21 gauge RMA flux.

All layer changing VIAs (PTHs) on the PCB to be filled with solder.

5.0 RCNW Circuit Diagram: Shown in fig:1.

The 44 pin J lead HMC 1461TP consists of 16 RCNetworks. All these networks have common ground pins. The filter time constant is 103µs.

6.0 Electrical Test Specifications & Electrical Test Procedure:

1. Measure the Resistance between I/P (pin nos: 2, 5, 8, 9, 14, 15, 18, 19, 24, 26, 29, 31, 37, 38, 41 & 42) and O/P (pin nos: 1, 6, 7, 10, 13, 16, 17, 20, 23, 27, 28, 32, 36, 39, 40 & 43) pins.

   Typical Value = 22 k Ω with a tolerance of 10%. The expected value is 19.8 k Ω to 24.2 k Ω.

2. Measure the capacitance between O/P (pin nos: 1, 6, 7, 10, 13, 16, 17, 20, 23, 27, 28, 32, 36, 39, 40 & 43) pins and Ground pins (pin no: 12 & 21).

   Typical Value = 4.7kpf with a tolerance of 10%. The expected value is 4.23kpf to 5.17kpf.

3. Give a pulse train of 500Hz, 1mSec pulse width, 5V to the I/P (pin nos: 2, 5, 8, 9, 14, 15, 18, 19, 24, 26, 29, 31, 37, 38, 41 & 42) and check all the sixteen O/P (pin nos: 1, 6, 7, 10, 13, 16, 17, 20, 23, 27, 28, 32, 36, 39, 40 & 43) pins.

   The settling time expected is ≈ 500-μsec±20% i.e. 400 to 600 μsec.
7.0 Block Diagram of Functional Test Jig:

Mechanical drawing of the YAMAICHI socket to be used in the test jig is given at the end of document 6.

8.0 RCNW O/P Monitoring

RCNW outputs are to be monitored during testing. Hence for this purpose suitable output monitoring sockets are to be provided on the front panel of the unit.

9.0 Monitoring of Input Signal

A suitable socket shall be provided in the front panel to monitor the input signal.

9.1 Supply Input & Monitoring

DC voltage of +5V is fed from external Power Supply. Hence suitable lamp post terminals shall be provided for the same.

Monitoring point, preferably terminal post shall be provided on the front panel for the power supply monitoring for +5V.
9.2 Interconnection Details:
The signal generation card and Yamaichi socket cards are to be interconnected and the connection details shall be incorporated in document.
The front panel selections and monitoring are to be wired from the signal generation card by adopting appropriate box wiring procedures.

9.3 Component List
Vendor shall procure all the materials for the realization of the test unit, including Yamaichi socket and MIL grade components.
Yamaichi socket shall be milled to accommodate the RCNW with ease and without disturbing the encapsulation of RCNW.

10.0 Deliverables by vendor
- Functional test unit
- All relevant documents
- Approved PCB L/Os all types
- Approved gerber files, component marking, PTH marking, drill detail prints
- Approved PCB film
- Box interconnection details
- Operation manual
- Hard copy in duplicate and soft copy in CD for the above details shall be provided.

11.0 Documentation:
As mentioned in the statement of work a detailed document both soft copy and hard copy shall be supplied as per the list given below:

Schematic diagrams
- PCB film details
- Component marking print
- PTH marking print
- Net list
- I/O details of each connector
- Box wiring details

12.0 Acceptance Criteria
Vendor should obtain acceptance from the Subsystem for the Circuit schematic diagram.
1. Bare PCB to be inspected by vendor's QA before mounting/ wiring of components. Initial electrical tests to be carried out at vendor's place only.
2. Only one unit shall be fabricated first and after obtaining the acceptance from subsystem and SRG for the same, subsequent units shall be fabricated.
3. The unit will be accepted after performance test in detail demonstrated at vendor's place and certified by the indenting subsystem and HQCS.
4. Vendor shall be ready to conduct the detailed demonstration at URSC if instructions are given for the same.
5. Vendor should strictly adhere to the delivery conditions as mentioned in P.O.
13.0 Rejection Criteria
The layout design or PCB or the unit as a whole will be rejected if it does not meet the required specifications as mentioned before. In case of any deviations in layout making, filming, PCB fabrication, wiring, testing the material, damages to the material supplied by URSC (if any) etc, the card or unit to be replaced free of cost by the vendor and replacement of unit/card should meet the specifications.

14.0 Secrecy
Vendor should not disclose or give details of the specifications in any form to anyone without the explicit permission from URSC. To this extent vendor has to execute a non-disclosure/secrecy agreement.

15.0 Warranty
All the items supplied to be warranted for a period of one year from the date of acceptance and any defective parts systems are to be replaced free of cost during warranty period.

Note: For the realization of the above work the guideline document is:

    STATEMENT OF WORK TO FABRICATE FUNCTIONAL TEST/BURN-IN TEST JIGS FOR TESTING HYBRID MICRO CIRCUITS

Unless specified in this indent guideline mentioned in the above documents are binding for the fabrication work.
SPECIFICATIONS FOR DESIGN, DEVELOPMENT AND FABRICATION OF BURN-IN JIG TO SCREEN 44PIN JLEAD RCNW1471LF

JULY 2019

U R RAO SATELLITE CENTRE
INDIAN SPACE RESEARCH ORGANISATION
BANGALORE
SPECIFICATIONS FOR DESIGN, DEVELOPMENT AND FABRICATION OF BURN-IN JIG TO SCREEN 44PIN JLEAD RCNW1471LF

1.0 GENERAL

Burn-in Jig consists of Burn-in unit, polyamide burn-in board and a harness to connect the burn-in board to burn-in unit. Realization of burn-in unit and burn-in board involves schematic entry, PCB layout design, filming, PCB fabrication, wiring of PCB, wiring of interface harness, integrated testing, housing of the electronic hardware in an appropriate mechanical package with aesthetic addition viz. screen printing, painting, etc. and supply of detailed operational and inter connection document.

2.0 Description of 44PIN JLEAD RCNW1471LF (See fig. 1)

1471LF is a RC filter network for processing analog channels with pull-down resistor before the filter. The filter time constant is 103μs. Single RC network contains 22 kΩ & 220 kΩ resistor with 4.7kpf capacitor. The 44 pin J lead RCNW1471LF consists of 16 RC networks.

All these networks have common ground pins.

3.0 Mechanical packaging details of 44PIN JLEAD RCNW1471LF (See Fig. 2 of Document 1)

<table>
<thead>
<tr>
<th>Description</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>No. of pins</td>
<td>44 pin</td>
</tr>
<tr>
<td>Substrate Size</td>
<td>0.65” x 0.65”</td>
</tr>
<tr>
<td>Overall Package size</td>
<td>0.67” x 0.67” without encapsulation</td>
</tr>
</tbody>
</table>

4.0 Work description:

The work involves development and fabrication of Burn-in unit, polyamide burn-in boards and connecting harnesses with proper document generation.

4.1.0 Description of RCNW Burn-in Unit

This unit should generate the required signals for the RCNWs. This unit should have a load resistor card to load outputs of the RCNWs. Burn-in configuration is provided in section 6.0. Also, provision shall be made for monitoring supplies, ground, inputs and total current drawn by the RCNWs.
Figure 2. Mechanical packaging details of 44PIN JLEAD RCNW 1461LF:
See the diagram in 1461LF document.

.1.1 Burn-in Unit consists of:
   a) Signal generation card.
   b) Interface connectors to burn-in PCB.
   c) Output loading resistor card.
   d) Monitoring sockets for i/p’s.
   e) RCNW current monitoring terminals.
   f) Monitoring of input signals.
   g) Supply I/P terminals and monitoring terminals.
   h) Power ON switch for +5V & +50V Supply.

.1.2 Burn-in Card:
The burn-in card should be designed so as to accommodate 12RCNWs in a single card. YAMAICHI sockets (Part No: IC51-0444-400) should be used to mount RCNWs on cards. These socket’s lids are to be milled to place the RCNW without damage. Four burn-in boards shall be used for a burn-in jig. Therefore, burn-in can be carried out on 48nos of 44 pin J Lead RCNWs 1461LF with single burn-in jig.

4.2 Document
A detailed document both soft copy and hard copy to be supplied as per the list given below:

- Schematic diagrams
- PCB film
- Gerber files for all layers
- Component marking print
- PTH marking print
- Net list
- I/O details of each connector
- Box wiring details

4.3 General Specifications for PCB Design (Two Layers only)
Following procedures are to be followed and approval from the Subsystem to be obtained for the final schematics diagram before proceeding to next stage. Inspection by the vendor’s internal QA to be carried out at various stages and report for the same in the format prescribed in the PMPD document (Doc No. INT: PMPD/SPES/HMC/GEN/13/REV-8) to be submitted along with the final unit.

4.3.1 General guidelines for Layout Design:
   No. Of layers: Two
   Following track widths are to be provided:
4.3.2 Filming
Filming has to be done with standard material of 7 MIL thick polymer based material. Contact film is not acceptable.

4.3.3 PCB Fabrication
d) PCB has to be fabricated using Polyamide board base material for Burn-in PCB and glass epoxy for PCBs in Burn-in test unit with thickness 1.6mm and solder masks with conformal coating and screen printing of component names to be done wherever required.
e) Bare Board Test (BBT) report to be furnished before wiring components on PCB.

4.3.4 PCB Wiring
As these PCBs are subjected to thermal cycling, the components are to be soldered using good quality solder; the part no. as mentioned below shall be used.

Spec./Part No. : 5 core, SN63PB37, 21 gauge RMA flux.

Additional external Flux shall not be used for wiring Burn-in PCBs.

All layer changing VIAs (PTHs) on the PCB to be filled with solder.

5.0 RCNW 1471 LF Circuit Diagram: Is given in fig:1

6.0 Burn-in configuration of 1471LF

Connection Details:
i) Short all Input (pin nos: 1, 6, 7, 10, 13, 16, 17, 20, 23, 27, 28, 32, 36, 39, 40 & 43) pins and Ground pins (pin no: 12 & 21) of all RCNWs and mark it as Low.
j) Short all output pins (pin nos: 2, 5, 8, 9, 14, 15, 18, 19, 24, 26, 29, 31, 37, 38, 41 & 42) of each RCNW, to this connect a 2.7 kΩ resistor one end; mark other end of 2.7 kΩ resistor as High.
k) Connect a 1 msec pulse (frequency-1kHz with 50% duty cycle) of amplitude 50V between High and Low points.

Test Duration:

<table>
<thead>
<tr>
<th>Sl.No.</th>
<th>Signal Description</th>
<th>Track Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Supply lines</td>
<td>40 MIL Min.</td>
</tr>
<tr>
<td>2.</td>
<td>Control signal lines</td>
<td>15 MIL Min.</td>
</tr>
<tr>
<td>3.</td>
<td>Spacing between tracks, pads, vias</td>
<td>12 MIL Min.</td>
</tr>
<tr>
<td>4.</td>
<td>Board edge to electrical components spacing</td>
<td>200 MIL Min.</td>
</tr>
</tbody>
</table>
96 hours at 70°C with a duty cycle of 1 ½ hours ON and ½ hour OFF.

6.1 **Burn-in Card:**

**A) Specifications for Burn-in Card Design**

- No. of 44pin RCNWs: 12 per PCB (Spacing for mounting **YAMAICHI** sockets to be provided) and 4 Burn-in cards
- PCB size: maximum 12” x 12”
- Input / Output: Amphenol connectors part nos given in SOW document
- Thickness of PCB: 1.6mm

**B) Layout Design:**

- No. of layers: Two
- Following track widths are to be provided:

<table>
<thead>
<tr>
<th>Sl.No.</th>
<th>Signal Description</th>
<th>Track Width</th>
</tr>
</thead>
<tbody>
<tr>
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<tr>
<td>4.</td>
<td>Board edge to electrical components spacing</td>
<td>200L min.</td>
</tr>
</tbody>
</table>

**C) Mechanical drawing of **YAMAICHI**(IC51-0444-400) Socket:** Is given at the end of this document.

6.2 **Output monitoring:**

**RCNW I/P & O/P Monitoring**

Input signals to RCNWs of 4 boards are to be monitored during course of testing. For this purpose, suitable monitoring points to be provided on the top panel.

**RCNW Current Monitoring**

Provision shall be made to connect one external Ammeters to monitor the current taken by individual burn-in PCB (12RCNWs). Hence provision shall be made to connect 4 current meters for 4 boards. Current drawn by the burn-in unit should not be included in any of these RCNW current monitoring.

**Supply Input & Monitoring**

DC voltage of +5V & +50V is fed from external Power Supply. Hence suitable lamp post terminals shall be provided for the same in the front panel.

Monitoring points for supplies and Gnd to be provided on the top panel.

6.3 **Harness and Connector Details:**

The part nos of connectors and specifications for wires provided in SOW are to be followed.

7.0 **Deliverables By Vendor**
Burn-in PCBs - As per indent
Burn-in test unit - As per indent
All relevant documents -
Approved PCB L/Os all types
Approved spool files, component marking, PTH marking, drill details prints
Approved PCB film
Unit interconnection details and Operation manual
Hard copy in duplicate and soft copy in CD for the above details shall be provided.

Interface test harness of length 2.2 meter – Qty. as per indent
Burn-in PCB photo film, layout, hard & soft copy for each of the PCB designed, developed or issued.

8.0 Documentation:
As mentioned in the statement of work a detailed document both soft copy and hard copy to be supplied as per the list given below:

- Schematic diagrams
- PCB film details
- Gerber files for all layers
- Component marking print
- PTH marking print&Net list
- I/O details of each connector
- Box wiring details

9.0 Acceptance Criteria

1. Vendor should obtain acceptance from the Subsystem for the Circuit schematic diagram.
2. Bare PCB to be inspected by vendor's QA before mounting/ wiring of components. Initial electrical tests to be carried out at vendor's place only.
3. Only one unit shall be fabricated first and after obtaining the acceptance from subsystem and HQCS for the same, subsequent units shall be fabricated.
4. The unit as a whole along with burn-in PCB, test unit and interface harness, will be accepted after performance test in detail demonstrated at vendor's place and certified by the indenting subsystem and HQCS.
5. Vendor shall be ready to conduct the detailed demonstration at URSC if instructions are given for the same.
6. Vendor should strictly adhere to the delivery conditions as mentioned in P.O.

10.0 Rejection Criteria
The layout design or PCB or the unit as a whole will be rejected if it does not meet the required specifications as mentioned before. In case of any deviations in layout making, filming, PCB fabrication, wiring, testing the material, damages to the material supplied by URSC (if any) etc, the card or
unit to be replaced free of cost by the vendor and replacement of unit/card should meet the specifications.

11.0 Secrecy
Vendor should not disclose or give details of the specifications in any form to anyone without the explicit permission from URSC. To this extent vendor has to execute a non-disclosure/secrecy agreement.

12.0 Warranty
All the items supplied to be warranted for a period of one year form the date of acceptance and any defective parts systems are to be replaced free of cost during warranty period.

Note: For the realization of the above work the guideline document is:

STATEMENT OF WORK TO FABRICATE FUNCTIONAL TEST/BURN-IN TEST JIGS FOR TESTING HYBRID MICRO CIRCUITS

Unless specified in this indent guideline mentioned in the above document are binding for the fabrication work.
SPECIFICATIONS FOR DESIGN, DEVELOPMENT AND FABRICATION OF FUNCTIONAL TEST JIG TO TEST/SCREEN 44PIN JLEAD RCNW1471LF

JULY 2019

U R RAO SATELLITE CENTRE
INDIAN SPACE RESEARCH ORGANISATION
BANGALORE
SPECIFICATIONS FOR DESIGN, DEVELOPMENT AND FABRICATION OF FUNCTIONAL TEST JIG TO TEST/SCREEN 44PIN JLEAD RCNW1471LF

1.0 GENERAL

Realization of functional test jig involves schematic entry, PCB layout design, filming, PCB fabrication, wiring of PCB, integrated testing, housing of the electronic hardware in an appropriate mechanical package with aesthetic addition viz. screen printing, painting, etc, box wiring and supply of detailed operational and inter connection document.

2.0 Description of 44PIN JLEAD RCNW1471LF (See Fig. 1)

1471LF is a RC filter network for processing analog channels with pull-down resistor before the filter. The filter time constant is 103µs. Single RC network contains 22 kΩ & 220 kΩ resistor with 4.7kpf capacitor. The 44 pin J lead HMC 1471LF consists of 16 RC networks. All these networks have common ground pins.

3.0 Mechanical packaging details of 44PIN JLEAD RCNW1471LF (See Fig. 2)

- No. of pins: 44 pin
- Substrate Size: 0.65” x 0.65”
- Overall Package size: 0.67” x 0.67” without encapsulation

4.0 Work description:

The work involves development and fabrication of functional test jig with proper document generation.

4.1 Description of J lead RCNW 1471 LF Functional Test Jig

This unit should provide interface for the necessary signals for the RCNW under test. Necessary input simulation signals are to be generated for simulating the inputs. Provision must be made to provide external signal. It also should have provision to connect or disconnect the input signal to input pins. Therefore, it is required to make int/ext switch for feeding internal/external stimuli. This unit should have front panel monitoring for the input simulation signal, RCNW inputs, outputs and ground.
Figure 1. Internal Circuit Diagram of 44PIN JLEAD RCNW1471LF
R1 - R16 = 22 kohms, ±10%, 20mW
R17 - R32 = 220 kohms, ±10%, 1mW
C1 - C16 = CDRO1/CDRO2 4.7KpF, ±10%, 100V
RN NO. 3, 12 & 21 = GND
PIN NO. 4, 11, 22, 25, 30, 33, 34, 35 & 44 = NC
Figure 2. Mechanical packaging details of 44PIN JLEAD RCNW1471LF: See 1451TP Document.
4.2 Functional Test Jig consists of:
   a) Signal generation card.
   b) YAMAICHI socket (part no: IC51-0444-400) card for placing the J Lead 44 pin RCNW during its functional test.
   c) Provision for RCNW I/P, O/P monitoring.
   d) Monitoring socket for simulation signal input.
   e) Supply and gnd.
   f) Power ON switch for +5 V Supply.

4.3 Document
A detailed document both soft copy and hard copy to be supplied as per the list given below:
- Schematic diagrams
- PCB film
- Component marking print
- PTH marking print
- Net list
- Front & back panel diagram of the box
- Box wiring details

4.4.0 General Specifications for PCB Design (Two Layers only)
Following procedures are to be followed and **approval from the Subsystem** to be obtained for the final schematics diagram before proceeding to next stage. Inspection by the vendor's internal QA to be carried out at various stages and report for the same in the format prescribed in the HQCS document (Doc No. INT: PMPD/SPES/HMC/GEN/13/REV-8) to be submitted along with the final unit.

4.4.1 General guidelines for Layout Design:
No. Of layers: Two
Following track widths are to be provided:

<table>
<thead>
<tr>
<th>Sl.No.</th>
<th>Signal Description</th>
<th>Track Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Supply lines</td>
<td>40 MIL Min.</td>
</tr>
<tr>
<td>2.</td>
<td>Control signal lines</td>
<td>15 MIL Min.</td>
</tr>
<tr>
<td>3.</td>
<td>Spacing between tracks, pads, vias</td>
<td>12 MIL Min.</td>
</tr>
<tr>
<td>4.</td>
<td>Board edge to electrical components spacing</td>
<td>200L Min.</td>
</tr>
</tbody>
</table>

4.4.2 Filming
Filming has to be done with standard material of 7 MIL thick polymer based material. Contact film is not acceptable.

4.4.9 PCB Fabrication

16.0 PCB has to be fabricated using glass epoxy with thickness 1.6mm and solder masks with conformal coating and screen printing of component names to be done wherever required.

17.0 Bare Board Test (BBT) report to be furnished before wiring components on PCB.

4.4.10 PCB Wiring

The components shall be soldered using good quality solder; the part number mentioned below shall be used.

Spec./Part No.: 5 core, SN63PB37, 21 gauge RMA flux.

All layer changing VIAs (PTHs) on the PCB to be filled with solder.

5.0 RCNW Circuit Diagram: Given in fig:1

The 44 pin J lead HMC 1471LF consists of 16 RC networks. All these networks have common ground pins. The filter time constant is 103µs.

6.0 Electrical Test Specifications & Electrical Test Procedure:

a. Measure the Resistance between I/P (pin nos: 2, 5, 8, 9, 14, 15, 18, 19, 24, 26, 29, 31, 37, 38, 41 & 42) and O/P (pin nos: 1, 6, 7, 10, 13, 16, 17, 20, 23, 27, 28, 32, 36, 39, 40 & 43) pins.
   Typical Value = 22 kΩ with a tolerance of 10%. The expected value is 19.8 kΩ to 24.2 kΩ.

b. Measure the Resistance between I/P (pin nos: 2, 5, 8, 9, 14, 15, 18, 19, 24, 26, 29, 31, 37, 38, 41 & 42) and Gnd (pin no: 3, 12 & 21) pins.
   Typical Value = 220 kΩ with a tolerance of 10%. The expected value is 198 kΩ to 242 kΩ.

c. Measure the capacitance between O/P (pin nos: 1, 6, 7, 10, 13, 16, 17, 20, 23, 27, 28, 32, 36, 39, 40 & 43) pins and Ground pins (pin no: 3, 12 & 21).
   Typical Value = 4.7kpf with a tolerance of 10%. The expected value is 4.23kpf to 5.17kpf.

d. Give a pulse train of 500Hz, 1mSec pulse width, 5V to the I/P (pin nos: 2, 5, 8, 9, 14, 15, 18, 19, 24, 26, 29, 31, 37, 38, 41 & 42) and check all the sixteen O/P (pin nos: 1, 6, 7, 10, 13, 16, 17, 20, 23, 27, 28, 32, 36, 39, 40 & 43) pins.
   The settling time expected is ≈ 500-µsec±20% i.e. 400 to 600 µsec.
6.1 Block Diagram of Functional Test Jig:

Mechanical drawing of the YAMAICHI socket to be used in the test jig is given at the end of this document.

6.2 RCNW O/P Monitoring

RCNW outputs are to be monitored during testing. Hence for this purpose suitable output monitoring sockets are to be provided on the front panel of the unit.

6.3 Monitoring of Input Signal

A suitable socket shall be provided in the front panel to monitor the input signal.

6.4 Supply Input & Monitoring

DC voltage of +5V is fed from external Power Supply. Hence suitable lamp post terminals shall be provided for the same.

Monitoring point, preferably terminal post shall be provided on the front panel for the power supply monitoring for +5V.
6.5 Interconnection Details:
The signal generation card and Yamaichi socket cards are to be interconnected and the connection details shall be incorporated in document. The front panel selections and monitoring are to be wired from the signal generation card by adopting appropriate box wiring procedures.

6.6 Component List
Vendor shall procure all the materials for the realization of the test unit, including Yamaichi socket and MIL grade components. Yamaichi socket shall be milled to accommodate the RCNW with ease and without disturbing the encapsulation of RCNW.

7.0 Deliverables by vendor
- Functional test unit
- All relevant documents
- Gerber files for all layers
- Approved PCB L/Os all types
- Approved spool files, component marking, PTH marking, drill detail prints
- Approved PCB film
- Box interconnection details
- Operation manual
- Hard copy in duplicate and soft copy in CD for the above details shall be provided.

8.0 Documentation:
As mentioned in the statement of work a detailed document both soft copy and hard copy shall be supplied as per the list given below:
- Schematic diagrams
  - PCB film details
  - Gerber files with all layers
  - Component marking print
  - PTH marking print
  - Net list
  - I/O details of each connector
  - Box wiring details
  - How to use the jig, etc.

9.0 Acceptance Criteria
1. Vendor should obtain acceptance from the Subsystem for the Circuit schematic diagram.
2. Bare PCB to be inspected by vendor's QA before mounting/wiring of components. Initial electrical tests to be carried out at vendor's place only.

3. Only one unit shall be fabricated first and after obtaining the acceptance from subsystem and HQCS for the same, subsequent units shall be fabricated.

4. The unit will be accepted after performance test in detail demonstrated at vendor's place and certified by the indenting subsystem and HQCS.

5. Vendor shall be ready to conduct the detailed demonstration at URSC if instructions are given for the same.

6. Vendor should strictly adhere to the delivery conditions as mentioned in P.O.

10.0 Rejection Criteria

The layout design or PCB or the unit as a whole will be rejected if it does not meet the required specifications as mentioned before. In case of any deviations in layout making, filming, PCB fabrication, wiring, testing the material, damages to the material supplied by URSC (if any) etc, the card or unit to be replaced free of cost by the vendor and replacement of unit/card should meet the specifications.

11.0 Secrecy

Vendor should not disclose or give details of the specifications in any form to anyone without the explicit permission from URSC. To this extent vendor has to execute a non-disclosure/secrecy agreement.

12.0 Warranty

All the items supplied to be warranted for a period of one year from the date of acceptance and any defective parts systems are to be replaced free of cost during warranty period.

Note: For the realisation of the above work the guideline document is:

STATEMENT OF WORK TO FABRICATE FUNCTIONAL TEST/BURN-IN TEST JIGS FOR TESTING HYBRID MICRO CIRCUITS

Unless specified in this indent guideline mentioned in the above documents are binding for the fabrication work.
SPECIFICATIONS FOR FABRICATION OF BURN-IN JIG TO SCREENRCNW 241TP

Description of RCNW: This 10 Pin Single-in-line package contains 4 identical Resistor Capacitor Networks (RCNW) with 10K and 15K resistor with 1Kpf Capacitor. This network is designed for Thermistor Processing and monitoring.

Mechanical Packaging Details:
No of pins : 10
Type of package : SIP (Single in line Package)
Overall Package size : 27.5x11.0x4.0 mm (Pin Pitch 2.54mm )

<table>
<thead>
<tr>
<th>RCNW PIN Number</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>VCC</td>
</tr>
<tr>
<td>2.</td>
<td>I/P-1</td>
</tr>
<tr>
<td>3.</td>
<td>O/P-1</td>
</tr>
<tr>
<td>4.</td>
<td>I/P-2</td>
</tr>
<tr>
<td>5.</td>
<td>O/P-2</td>
</tr>
</tbody>
</table>
### 241TP BURN-IN TEST SPECIFICATIONS

<table>
<thead>
<tr>
<th>HMC Pin No</th>
<th>Function</th>
<th>Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>VCC</td>
<td>100µsec (with 25% duty cycle) @ 50V</td>
</tr>
<tr>
<td>2.</td>
<td>I/P-1</td>
<td>100µsec (with 25% duty cycle) @ 50V</td>
</tr>
<tr>
<td>3.</td>
<td>O/P-1</td>
<td>GND</td>
</tr>
<tr>
<td>4.</td>
<td>I/P-2</td>
<td>100µsec (with 25% duty cycle) @ 50V</td>
</tr>
<tr>
<td>5.</td>
<td>O/P-2</td>
<td>GND</td>
</tr>
<tr>
<td>6.</td>
<td>I/P-3</td>
<td>100µsec (with 25% duty cycle) @ 50V</td>
</tr>
</tbody>
</table>
1. Connect the Power Supplies and current meters as shown in the box panel details.
2. Set the power supplies to 50V/2.5A and 5V/0.25A.
3. Connect the Burn-in Card through harness to the Burn-in-Unit.
4. Switch on the power supplies and jig without inserting device.
5. Check for the I/P Signal of 100µsec (25% duty cycle) with 50V amplitude at the monitoring sockets of the burn-in unit and sockets on all four burn-in boards.
6. When the I/P is present in all 4 rows (front panel marked as IP1,IP2,IP3 & IP4) and burn-in boards, switch off the jig and mount the RCNWs.
7. Switch ON 50V & 5V power supply one after another in the jig.
8. Check for the RCNW outputs and current drawn by RCNWs. Monitor and record all the readings.
9. Compare the recorded readings with the test results and waveforms attached with this document at the end.

### 241TP BURN-IN CONFIGURATION

<table>
<thead>
<tr>
<th>HMC Pin No</th>
<th>Function</th>
<th>Signal to be applied</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VCC</td>
<td>100µsec (with 25% duty cycle) @ 50V (to be applied)</td>
</tr>
<tr>
<td>2</td>
<td>I/P-1</td>
<td>100µsec (with 25% duty cycle) @ 35V (monitoring)</td>
</tr>
<tr>
<td>3</td>
<td>O/P-1</td>
<td>GND</td>
</tr>
<tr>
<td>4</td>
<td>I/P-2</td>
<td>100µsec (with 25% duty cycle) @ 35V (monitoring)</td>
</tr>
<tr>
<td>5</td>
<td>O/P-2</td>
<td>GND</td>
</tr>
<tr>
<td>6</td>
<td>I/P-3</td>
<td>100µsec (with 25% duty cycle) @ 35V (monitoring)</td>
</tr>
<tr>
<td>7</td>
<td>O/P-3</td>
<td>GND</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>---</td>
<td>---</td>
<td>---</td>
</tr>
<tr>
<td>8</td>
<td>I/P-4</td>
<td>100µsec (with 25% duty cycle) @ 35V (monitoring)</td>
</tr>
<tr>
<td>9</td>
<td>O/P-4</td>
<td>GND</td>
</tr>
<tr>
<td>10</td>
<td>GND</td>
<td>GND</td>
</tr>
</tbody>
</table>

**241TP BURN-IN JIG BLOCK DIAGRAM**

INPUT & OUTPUT MONITORING SOCKETS

EXTERNAL POWER SUPPLY (50V & 5V)

SIMULATOR UNIT
WITH BUILT-IN SIGNAL GENERATOR

INTERFACE HARNESS

4 BURN-IN CARDS IN A STACK

**FRONT PANEL CONSIST OF**

1. **4 CURRENT METERS** — EACH METER FOR 1 BURN-IN CARD
2. **4 I/P MONITORING SOCKET** — ONE I/P TO EACH BURN-IN CARD
3. **64 O/P MONITORING SOCKET** — 4 O/Ps FOR EACH ROW OF RCNWs
   - 4 ROWS FOR EACH BURN-IN CARD & FOUR CARDS
### TOP PANEL

**ISRO SATELLITE CENTRE - BANGALORE**

241TP BURN-IN TEST JIG  
241TP 07 BIJ 001

<table>
<thead>
<tr>
<th>INPUTS</th>
<th>5Vpp</th>
<th>50Vpp</th>
<th>IP1</th>
<th>IP2</th>
<th>IP3</th>
<th>IP4</th>
</tr>
</thead>
<tbody>
<tr>
<td>BOARD-1</td>
<td>A1</td>
<td>A2</td>
<td>A3</td>
<td>A4</td>
<td>B1</td>
<td>B2</td>
</tr>
<tr>
<td></td>
<td>C1</td>
<td>C2</td>
<td>C3</td>
<td>C4</td>
<td>D1</td>
<td>D2</td>
</tr>
<tr>
<td>BOARD-2</td>
<td>A1</td>
<td>A2</td>
<td>A3</td>
<td>A4</td>
<td>B1</td>
<td>B2</td>
</tr>
<tr>
<td></td>
<td>C1</td>
<td>C2</td>
<td>C3</td>
<td>C4</td>
<td>D1</td>
<td>D2</td>
</tr>
<tr>
<td>BOARD-3</td>
<td>A1</td>
<td>A2</td>
<td>A3</td>
<td>A4</td>
<td>B1</td>
<td>B2</td>
</tr>
<tr>
<td></td>
<td>C1</td>
<td>C2</td>
<td>C3</td>
<td>C4</td>
<td>D1</td>
<td>D2</td>
</tr>
<tr>
<td>BOARD-4</td>
<td>A1</td>
<td>A2</td>
<td>A3</td>
<td>A4</td>
<td>B1</td>
<td>B2</td>
</tr>
<tr>
<td></td>
<td>C1</td>
<td>C2</td>
<td>C3</td>
<td>C4</td>
<td>D1</td>
<td>D2</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>OUTPUTS</th>
<th>5V</th>
<th>50V</th>
</tr>
</thead>
<tbody>
<tr>
<td>K1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>K2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>K3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>K4</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### FRONT PANEL

- **5V**  
  - SUPPLY
- **50V**  
  - GND
- **5V** ON  
  - OFF
- **5Vpp**  
  - 50Vpp
- CURRENT MONITORING
SPECIFICATIONS FOR FABRICATION OF BURN-IN JIG TO SCREEN RCNW 147LF

This 10 Pin Single-in-line package contains 4 identical Resistor Capacitor Networks (RCNW) with 220KΩ pull down, 22KΩ resistor with 4.7KPF Capacitor and series 2.2KΩ resistor. This network is used as Input filter for all analog inputs to BMU.

Mechanical Packaging Details:

No of pins : 10
Type of package : SIP (Single in line Package)
Overall Package size : 27x11x4 mm (Pin Pitch 2.54mm)

147LF RCNW PIN CONFIGURATION

<table>
<thead>
<tr>
<th>HMC PIN Number</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>NC</td>
</tr>
<tr>
<td>2</td>
<td>I/P-1</td>
</tr>
<tr>
<td>3</td>
<td>O/P-1</td>
</tr>
<tr>
<td>4</td>
<td>I/P-2</td>
</tr>
<tr>
<td>5</td>
<td>O/P-2</td>
</tr>
<tr>
<td>6</td>
<td>I/P-3</td>
</tr>
</tbody>
</table>
Description:
This 10 pin single in line package contains 4 identical RC network with 220K pull down 22 K resistor with 4.7KPF capacitor and series 2.2K resistor.

Specification:
- Input range: ±5V
- Filter time constant: 103.4 µsec
- Absolute max: 50V

Application:
This RC network is used as input filter for all analog inputs to BMU.

Test Procedure:
1) Measure the resistance from I/Ps (at 2, 4, 6, & 8) to individual O/P (pins 3, 5, 7 & 9) expected value (≈ 24.2K ±10%)
2) Measure the resistance from I/Ps (at 2, 4, 6, & 8) to GND. expected value 220K ±10%.
3) Measure the capacitance between O/P (pin 3, 5, 7 & 9) and GND.
4) Give a pulse train of 500Hz, 1msec PW, 5V to the I/P and check all the four O/P (settling time ≈ 500 µsec ±20%).
147LF (100 μsec)

<table>
<thead>
<tr>
<th>NC</th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td>I/P</td>
<td>2</td>
</tr>
<tr>
<td>O/P</td>
<td>3</td>
</tr>
<tr>
<td>I/P</td>
<td>4</td>
</tr>
<tr>
<td>O/P</td>
<td>5</td>
</tr>
<tr>
<td>I/P</td>
<td>6</td>
</tr>
<tr>
<td>O/P</td>
<td>7</td>
</tr>
<tr>
<td>I/P</td>
<td>8</td>
</tr>
<tr>
<td>O/P</td>
<td>9</td>
</tr>
<tr>
<td>GND</td>
<td>10</td>
</tr>
</tbody>
</table>

10 PIN RC NETWORK SIP

R1=22K–20mW–10%
R2=2.2K–20mW–10%
R3=220K–1mW–10%
C1=4.7kpf–100v–20%
147LF BURN-IN TEST SPECIFICATIONS

Supply Voltages: + 5V & + 50V
Test temperature: 70°C
Test Duration: 96hours; 90 minutes ON & 30minutes OFF
Expected current: 43.5 to 4.5 mA/RCNW

147LF BURN-IN CONFIGURATION

<table>
<thead>
<tr>
<th>HMC Pin No</th>
<th>Function</th>
<th>Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>NC</td>
<td>NC</td>
</tr>
<tr>
<td>2</td>
<td>I/P-1</td>
<td>GND</td>
</tr>
<tr>
<td>3</td>
<td>O/P-1</td>
<td>Pulse width 1msec (With 50% duty cycle), 500 Hz, @ 50V</td>
</tr>
<tr>
<td>4</td>
<td>I/P-2</td>
<td>GND</td>
</tr>
<tr>
<td>5</td>
<td>O/P-2</td>
<td>Pulse width 1msec (With 50% duty cycle), 500 Hz, @ 50V</td>
</tr>
<tr>
<td>6</td>
<td>I/P-3</td>
<td>GND</td>
</tr>
<tr>
<td>7</td>
<td>O/P-3</td>
<td>Pulse width 1msec (With 50% duty cycle), 500 Hz, @ 50V</td>
</tr>
<tr>
<td>8</td>
<td>I/P-4</td>
<td>GND</td>
</tr>
<tr>
<td>9</td>
<td>O/P-4</td>
<td>Pulse width 1msec (With 50% duty cycle), 500 Hz, @ 50V</td>
</tr>
<tr>
<td>10</td>
<td>GND</td>
<td>GND</td>
</tr>
</tbody>
</table>

147LF BURN-IN TEST PROCEDURE

2. Connect the Burn-in Card through harness to the Burn-in-Unit.
3. Check for the I/P Signal of 1msec (50% duty cycle) at amplitude 50V.
4. When the I/P is present in all 4 rows (front panel marked as IP1, IP2, IP3 & IP4), “Switch OFF” and mount the RCNWs.
5. “Switch ON” 50V & 5V power supply one after another and Unit power – ON switch.
6. Check for the current per RCNW and current per RCNW shall 4mA.
147LF BLOCK DIAGRAM OF BURN-IN SYSTEM

FRONT PANEL CONSIST OF
1. 4 CURRENT METERS ----- EACH METER FOR 1 BURN-IN CARD
2. 4 1P MONITORING SOCKET ----- ONE UP TO EACH BURN-IN CARD
Yamaichi Data sheet

IC51 Series (Clamshell) Plastic Lead Chip Carrier (PLCC)

Specifications
Insulation Resistance: 1,000MΩ min. at 500V DC
Dielectric Withstanding Voltage: 700V AC for 1 minute
Contact Resistance: 30mΩ max. at 10mA/20mV max.
Current Rating: 1A max.
Operating Temperature Range: -55°C to +170°C
Mating Cycles: 10,000 Insertions min.

Materials and Finish
Housing: Polyether sulfone (PES), glass-filled
Contacts: Beryllium Copper (BeCu)
Plating: Gold over Nickel

Features
- Clamshell socket for PLCC packages

Outline Socket Dimensions

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Pin Count</th>
<th>Pitch</th>
<th>A</th>
<th>B</th>
<th>C (open)</th>
<th>D (closed)</th>
</tr>
</thead>
<tbody>
<tr>
<td>IC51-0204-602</td>
<td>20</td>
<td>1.27</td>
<td>31.5</td>
<td>26.0</td>
<td>10.0</td>
<td>20.0</td>
</tr>
<tr>
<td>IC51-0234-299</td>
<td>28</td>
<td>1.27</td>
<td>36.0</td>
<td>20.0</td>
<td>10.0</td>
<td>20.5</td>
</tr>
<tr>
<td>IC51-0234-452</td>
<td>32</td>
<td>1.27</td>
<td>35.0</td>
<td>30.0</td>
<td>9.0</td>
<td>19.5</td>
</tr>
<tr>
<td>IC51-0444-400</td>
<td>44</td>
<td>1.27</td>
<td>40.0</td>
<td>34.0</td>
<td>10.0</td>
<td>20.0</td>
</tr>
<tr>
<td>IC51-0524-411-1</td>
<td>52</td>
<td>1.27</td>
<td>43.0</td>
<td>36.0</td>
<td>10.0</td>
<td>22.5</td>
</tr>
<tr>
<td>IC51-0624-390-1</td>
<td>68</td>
<td>1.27</td>
<td>49.0</td>
<td>42.0</td>
<td>10.0</td>
<td>23.5</td>
</tr>
<tr>
<td>IC51-0844-401-1</td>
<td>84</td>
<td>1.27</td>
<td>55.0</td>
<td>46.0</td>
<td>10.0</td>
<td>23.5</td>
</tr>
<tr>
<td>IC51-1004-405-1</td>
<td>100</td>
<td>1.27</td>
<td>60.6</td>
<td>54.0</td>
<td>10.0</td>
<td>23.5</td>
</tr>
<tr>
<td>IC51-1244-410-1</td>
<td>124</td>
<td>1.27</td>
<td>65.0</td>
<td>60.0</td>
<td>10.0</td>
<td>23.5</td>
</tr>
</tbody>
</table>
STATEMENT OF WORK TO FABRICATE FUNCTIONAL TEST/ BURN-IN TEST JIGS FOR TESTING HYBRID MICRO CIRCUITS & RC NETWORKS

July 2019

COMPONENTS MANAGEMENT GROUP
U R RAO SATELLITE CENTRE
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   4.2. Responsibility of Vendor
5.0. Facility & Personnel Requirements
6.0. Working Modality
7.0. Deliverables
8.0. Acceptance Criteria
9.0. Rejection Criteria
10.0. Secrecy
11.0. Applicable Documents
12.0. Warranty
13.0. Quotation details

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Appendix – 1: Definition of Jigs
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STATEMENT OF WORK TO REALIZE FUNCTIONAL TEST/ BURN-IN TEST JIGS FOR TESTING HYBRID MICRO CIRCUITS (RCNWs)

1.0. SCOPE: - This document gives the statement of work for realizing the Functional test Jigs/ burn-in Jigs used for testing and carrying out burn-in of flight Hybrid Micro Circuits (HMCs) & RCNWs.

2.0. INTRODUCTION: - As large number of HMCs/RCNWs are being used on board satellites, the need for fabricating more and more Jigs also increased. This document gives the total work involved in realizing the Jigs and the identification of responsibilities in detail. The definition of Functional Test Jig, Burn-in Jig and serialization of Jigs are given in Appendix –1.

3.0. DESCRIPTION OF THE WORK: - The vendor shall be responsible for realization of Functional test/ Burn-in Jig as per the requirements spelt out in Appendix 2 and Appendix 3. After the fabrication and assembly, the jig shall be offered to HQCS for approval along with vendor’s QC Inspection Report. The format for QC Inspection Report is given in Appendix-4. The fabricated and tested Functional test Jig/ Burn-in Jig shall be delivered to URSC, along with the associated documents. The documents shall contain the details as per the checklists provided in Appendix 5 and Appendix 6.

4.0. RESPONSIBILITY DEFINITION

4.1. RESPONSIBILITY OF URSC: -

- Description of HMC/RCNW to the vendor for the purpose of realising the document.
- To provide the approved Electrical Test Specifications (to realise Functional test jig). Also to provide the approved burn-in configuration, approved burn-in test specifications (to realise Burn-in test jig).
- To provide the Burn-in configuration of HMC/RCNW to Vendor.
To provide the requirements of powering, monitoring and measurement of Functional test jig / Burn-in test jig.

Respective Subsystem is required to approve the electrical design of test jig/Burn-In Jig to carry out the Functional test/Burn-In test of HMC/RCNW for their adequacy and accuracy to meet the test specifications.

To approve the bill of materials as per the formats given in Tables 4, 5 and 6 and check the certificate of conformance for all materials.

- To arrange training for two people from each vendor for 2, 3 days for general aspects of fabrication including conformal coating of burn-in boards. -- HQCS
- To provide necessary clarification as and when required.
- Check whether the QC Inspection report, documents are submitted along with the Jig for evaluation.
- To ensure that all the documentation in the suggested formats is supplied with the Jigs and is as per the requirements / specifications.
- The vendor shall test the jig for its complete specifications in the presence of concerned subsystem engineer & HQCS engineer. In case of burn-in jig it is mandatory to check all the slots with master HMC/RCNW.
- The subsystem and HQCS engineer shall accept the jig jointly.

4.2. RESPONSIBILITY OF VENDOR:

- To provide the design for realising the Functional test jig as per specifications and to get the approval from subsystem. The mechanical design of the functional jig should be approved by both subsystem and HQCS.
- To provide the design for realising the burn-in test jig as per the burn-in configuration and burn-in test specifications and to get the approval from subsystem. The mechanical design of the burn-in jig should be approved by both subsystem and HQCS.
- To procure the required material as per specifications listed in Table-3 and use the material as per the requirements given in Table-1 and Table-2. To provide the Bill of Materials (BOM) for subsystem approval and provide the approved BOM in the document along with the deliverables.
Vendor QC shall make sure that the approved design and correct values of components are only used for the fabrication of Jigs.

To carry out the fabrication and assembly work only by the trained and qualified operators. Only one unit shall be fabricated at first. The proto Jig shall be evaluated thoroughly by URSC team (Subsystem + HQCS) and one-week ambient burn-in should be performed on proto unit. After getting approval for proto Jig, the fabrication of production units must be initiated. At least one-day ambient burn-in shall be performed on all production BIJs and the results of all BIJs shall be enclosed in all BOJ manuals.

To prepare and submit the documents as per the checklists given in Appendix 4 & 5.

To give the conformal coating to the burn-in board as per the guidelines given in Appendix-3.

5. FACILITY & PERSONNEL REQUIREMENTS FOR CARRYING OUT FUNCTIONAL/ BURN-IN JIG FABRICATION:

a) The facility shall have necessary features like

- Sufficient PWB Assy. area with ESD schemes
- PWB testing facility with all the required equipment.
- Fabrication tools -- as listed in document “QC Guidelines For Fabrication of Ground Support Equipment.
  Doc. No. URSC – 32-93-08-05-06.”
- Vendors shall identify the jobs that are subcontracted by them with all necessary details.

b) The vendor shall give details of technical manpower, availability of lab facilities and previous experience along with the proposal. The operators shall be well trained and must be qualified (at least two) by HQCS. The vendor shall employ personnel with a qualification of at least a diploma in Electronics for testing purposes.
6.0. **WORKING MODALITY:** Vendor shall identify a senior employee as a focal point who shall interact with URSC for all related matters. Indentor shall be the focal point from URSC.

7.0. **DELIVERABLES:**

1. Jig
2. Document
3. QC Inspection Report
4. Bill of Materials (in the specified formats)
5. Warranty Certificate
6. i) Approved PCB Layouts of all PCBs, Gerber files for all layers like Component Marking, PTH marking, drilling details prints
   ii) Approved PCB Film
   iii) Unit Interconnection Details

The details mentioned in (6) above shall be submitted in hard copy and soft copy in DVD.

8.0. **ACCEPTANCE CRITERIA:**

Vendor shall obtain the inspection and acceptance for the following details:

i) Inspection/ Audit by HQCS, URSC (Vendor shall provide internal QC Inspection Report)
ii) Electrical Functionality check
iii) Burn-In tests/Evaluation tests on Jigs at the vendor site.
iv) Documentation + Fabrication Folder
v) Conformal Coating (in case of burn-in board)
vi) Serialization

In addition to the above the vendor shall obtain approvals as per the flowcharts given in Appendix-2 & 3. The fabrication folder shall consist of the measured values of all components (along with their ratings as per the format given in Table-7) and all rework/repair details.
The unit as a whole along with burn-in PCB, test unit and interface harness will be accepted after testing in detail at Vendor’s premises and certified by indenter in the presence of concerned subsystem and HQCS engineers. Only after evaluating and accepting one burn-in jig, the remaining quantity (in purchase order) of burn-in Jigs shall be fabricated.

9.0. REJECTION CRITERIA: -
The layout design or PCB or the unit as a whole shall be rejected if it does not confirm to the required specifications as provided in the indent. In case of any deviations the card or unit to be replaced free of cost by the vendor and replacement of unit/card should meet the specifications.

10.0. SECRECY: -
Vendor shall not disclose or give details of the specifications in any form to any one without the explicit permission from URSC. To this extent vendor has to execute a non-disclosure/secrecy agreement.

11.0. WARRANTY: -
All the items supplied to be warranted for a period of one year from the date of acceptance and any defective parts/systems are to be replaced free of cost during warranty period.

12.0. APPLICABLE DOCUMENTS: -
QC Guidelines for Fabrication of Ground Support Equipment
Doc. No. URSC – 32-93-08-05-06

13.0. Quotations should include following details:
   a) Material Cost: Should include the split up for each item.
   b) Fabrication Cost: Should include the split up for each activity.
   c) Testing and Validation Charges.
   d) Non Recurring Engineering Cost: Should include the split up for each activity.
   e) Any other.
Definition of Functional Test Jig: - It consists of signal generation, monitoring and load circuitry assembled in a box with a suitable (ZIF/Azimuth/Yamaichi) socket. At a time one HMC/RCNW can be tested for its functionality.

Definition of Burn-In Jig: - It consists of Burn-In Unit, Burn-In Board/s and Harnesses (with connectors on either side) to have the connectivity between Burn-In unit and Burn-In Boards.

Burn-In Unit: - It consists of signal generation circuitry, monitoring circuitry and load cards etc. assembled in a box. The front and or back panel of the box contain the connectors. In case of few circuits like relay drivers the signal generator circuitry and load circuitry are also stacked and separate units are made. Therefore, in such cases the Burn-In unit is divided into Signal Generation unit and Load unit.

Burn-In Board/s: - Usually Jigs will have one or two burn-in boards. In very few circuits like relay drivers, the burn-in boards are stacked and are referred as stacked burn-in boards.

Serialization of Jigs: - The serial number shall be engraved on the Functional test jig, burn-in unit as well as on the burn-in boards as per the guidelines given below.

It is a 13-digit code for Functional test jig and Burn-in unit where as it is a 14-digit code for burn-in boards.

```
XXXXX XX XXX XXX/X
```

First 5 digits specify the HMC/RCNW type. Eg: 222DM
Digits 6 & 7 specify the year of accepting the jig. Eg: 03
Digits 8,9 & 10 specify the type of jig.
If it is Functional test jig, it shall be mentioned as **FTJ**
If it is burn-in jig, it shall be mentioned as **BIJ**

Digits 11, 12 & 13 specify the **serial number of the jig**.

Eg: **001** or **090**.
Digit 14 specifies the **serial number of the board** attached to that particular jig. Eg: **1, 2 or n (n is the no. of boards in a stack)**.

Eg. Of 13-digit code: **222DM 03 FTJ 005**.
Eg. Of 14-digit code: **222DM 03 BIJ 005/2**

The bunch of harnesses must be labelled with serial No. of the Burn-In Jig.
REQUIREMENT SPECIFICATION FOR REALISING FUNCTIONAL TEST JIG

Sequence of operations for realizing the Functional Test Jig:

1. Vendor shall get the complete requirements like HMC/RCNW circuit description, HMC/RCNW pin configuration, Functional test specifications from subsystem for making the Functional test jig.

2. Vendor shall make the design for realizing the Functional test jig as per the test specifications and get the approval from subsystem engineer (when the design is done by vendor). The design includes generation of input signals, clock and or address signals, and monitoring and load circuitry.

3. Vendor shall procure the material as per the specifications given in Table-3. Make sure that only the material specified in Table-1 is used. Vendor shall submit the bill of materials to the subsystem. The subsystem shall ensure that the materials procured are of required quality and are as per the subsystem-approved design (in step2).

4. Vendor shall make the layout design as per the document “QC Guidelines For Fabrication of Ground Support Equipment. Doc. No. URSC – 32-93-08-05-06”. The subsystem shall mention the specific layout requirements (if any) in the indent.

5. Vendor shall submit the layout design for their internal QC approval. Vendor’s internal QC shall ensure that this design is as per the subsystem-approved design (in step2).

6. Subsystem shall make sure that the types and precise values of components specified are only used. Make sure that mechanical guide lines as given in Table-2 and as per the document “QC Guidelines for Fabrication of Ground Support Equipment. Doc. No. URSC – 32-93-08-05-06” are followed.
7. The Jig shall be inspected by the internal QC of the vendor and generate a report as per the format given in Appendix-4. Vendors shall obtain the approval of HQCS for fabrication completeness.

8. The Jig shall be tested for the test specifications without HMC/RCNW. After making sure that all signals are as specified, the Jig shall be tested with a master HMC/RCNW.

9. Vendor shall make the document as per the checklists given in Appendix 3 and 4.

10. With approved QC Inspection Report, the Jig shall be offered to URSC along with the associated document and with bill of materials for inspection and testing. HQCS and subsystem are jointly responsible for accepting the Jig”.

11. All the tests shall be carried out at Vendor’s site. Acceptance of Jig shall be done at URSC.
APPENDIX – 3

REQUIREMENT SPECIFICATION FOR REALISING BURN-IN TEST JIG

Sequence of operations in realizing the Burn-In Jig:

1. Vendor shall get the complete requirements like the HMC/RCNW circuit description, HMC/RCNW pin configuration, Burn-in test specifications from subsystem for making the burn-in test jig.

2. Vendor shall make the design for realizing the burn-in test jig as per the burn-in configuration and test specifications. The design includes generation of input signals, clock and or address signals, and monitoring circuitry and load circuitry. Vendor shall get the design approved from subsystem engineer.

3. Vendor shall procure the material as per the specifications given in Table-3. Make sure that only the material specified in Table-1 is used. Vendor shall submit the bill of materials to the subsystem. The subsystem shall ensure that the materials procured of required quality and are as per the subsystem-approved design (in step2).

4. Vendor shall make the layout design as per the document “QC Guidelines for Fabrication of Ground Support Equipment” Doc. No. URSC – 32-93-08-05-06. The test pattern drawing for making test coupon (along with the burn-in PCB) is enclosed in figure 1. The burn-in card shall be realized only in double-sided PCB. HQCS shall provide the spool file for test coupon to the vendor. Subsystem shall mention the specific layout requirements (if any) in the indent.

5. Vendor shall submit the layout design for their internal QC approval. Vendor’s internal QC shall ensure that this design is as per the subsystem-approved design (in step2).
6. Vendor shall fabricate the burn-in jig. Subsystem shall make sure that the types and precise values of components specified are only used. Make sure that mechanical guide lines as given in Table-2 and as per the document “QC Guidelines for Fabrication of Ground Support Equipment. Doc. No. URSC – 32-93-08-05-06.”

7. The Jig shall be inspected by the internal QC of the vendor and generate a report as per the format given in Appendix-4. Vendors shall obtain the approval of HQCS for fabrication completeness.

8. The Jig shall be tested for the test specifications without HMC/RCNW. After making sure that all signals are as specified, all slots of the burn-in board shall be tested with master HMC/RCNW.

9. Vendor shall make the document as per the checklists given in Appendix 3 & 4.

11. The connectors of harnesses of burn-in jig must be potted (potting material- RTV3145) both sides. Before potting ensure that one to one electrical connections are made properly.

12. All the tests shall be carried out at Vendor’s site. Acceptance of Jig shall be done at URSC.

13. With approved QC Inspection Report, the Jig shall be offered to URSC along with the associated document and with bill of materials for inspection and testing. HQCS and subsystem are jointly responsible for accepting the jig.
UR RAO SATELLITE CENTRE
COMPONENTS QUALITY CONTROL DIVISION
HMC QUALITY CONTROL SECTION

INSPECTION REPORT

REF. NO.                      DATE:

PRODUCT: - BURN-IN BOARD/ BURN-IN JIG/ FUNCTIONAL TEST
          JIG/ CONNECTOR HARNESS

NOMENCLATURE:
SERIAL NUMBER:

<table>
<thead>
<tr>
<th>SL. NO.</th>
<th>OPERATIONS</th>
<th>INSPECTION STATUS</th>
<th>REWORKS IF ANY</th>
<th>APPROVED</th>
<th>REMARKS</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PCB LAYOUT</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>PCB MASTER FILM</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>BARE PCB</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>COMPONENTS MOUNTING</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>COMPONENTS SOLDERING</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>HARNESS ROUTING</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>HARNESS WIRE SOLDERING</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>LACING</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>CLEANING</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>MECHANICAL ASSEMBLY</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>DOCUMENT</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>OTHERS</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

THIS PRODUCT IS CHECKED AND CLEARED FOR INSPECTION TO URSC

CHECKLIST FOR FUNCTIONAL TEST JIG DOCUMENT
FUNCTIONAL TEST JIG DOCUMENT SHALL CONTAIN THE FOLLOWING DETAILS:

<table>
<thead>
<tr>
<th>SL. NO.</th>
<th>NAME OF THE DETAIL</th>
<th>PAGE NO.</th>
<th>REMARKS</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>INTRODUCTION</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>DESCRIPTION OF HMC/RCNW</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>HMC/RCNW PIN CONFIGURATION -MECHANICAL DIMENSIONS</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>HMC/RCNW CIRCUIT DIAGRAM</td>
<td></td>
<td>*It will be given to vendor @ URSC for inclusion in document.</td>
</tr>
<tr>
<td>5</td>
<td>ELECTRICAL TEST SPECIFICATIONS</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>ELECTRICAL TEST PROCEDURE</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>FABRICATION DETAILS OF THE FOLLOWING A) FRONT PANEL B) BACK PANEL C) TOP PANEL</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>INTERNAL VIEW OF THE JIG &amp; BLOCK DIAGRAM OF TOTAL FTJ</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>TOTAL CIRCUIT DIAGRAM OF FTJ (INCLUDING SIGNAL GENERATION &amp; LOAD CIRCUITRY)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>INDIVIDUAL PCB CIRCUIT DIAGRAM WITH COMPONENT DETAILS</td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>LAYOUT DIAGRAMS OF INDIVIDUAL PCBs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>INTERNAL CONNECTION DETAILS BETWEEN PCBs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>INTERNAL CONNECTION DETAILS BETWEEN PCBs AND DIFFERENT (FRONT, BACK, TOP ETC.) PANELS</td>
<td></td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>BILL OF MATERIALS, <strong>TEST RESULTS (along with all Input/Output waveforms)</strong> OF ONE HMC/RCNW &amp; FABRICATION FOLDER</td>
<td></td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>WARRANTY CERTIFICATE</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

APPENDIX –5

CHECKLIST FOR BURN IN TEST JIG DOCUMENT

BURN IN TEST JIG DOCUMENT SHALL CONTAIN THE FOLLOWING DETAILS:

- **TEST RESULTS** (along with all Input/Output waveforms)
- BILL OF MATERIALS
<table>
<thead>
<tr>
<th>Sl.No.</th>
<th>NAME OF THE DETAIL</th>
<th>PAGE NO.</th>
<th>REMARKS</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>INTRODUCTION</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>DESCRIPTION OF HMC /RCNW</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>HMC/RCNW PIN CONFIGURATION - MECHANICAL DIMENSIONS</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>HMC/RCNW CIRCUIT DIAGRAM</td>
<td></td>
<td>*It will be given to vendor @ URSC for inclusion in document.</td>
</tr>
<tr>
<td>5</td>
<td>BURN IN TEST SPECIFICATIONS</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>BURN IN TEST PROCEDURE</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>BURN IN CONFIGURATION DETAILS EACH HMC/RCNW PIN – CONNECTION DETAILS</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>BLOCK SCHEMATIC OF TOTAL BURN-IN SYSTEM &amp; TOTAL CIRCUIT DIAGRAM OF BIJ (INCLUDING SIGNAL GENERATION &amp; LOAD CIRCUITRY)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>GENERATOR CARD LAYOUT, CIRCUIT AND COMPONENT DETAILS</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>BURN IN CARD LAYOUT, CIRCUIT AND COMPONENT DETAILS</td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>DISPLAY OR OUTPUT MONITORING PART – FRONT PANEL AND/OR TOP PANEL DETAILS</td>
<td></td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>HARNESS AND CONNECTOR DETAILS</td>
<td></td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>INTER CONNECTION DETAILS OF THE FOLLOWING A) BETWEEN BURN IN CARD AND GENERATOR CARD B) BETWEEN BURN IN CARD AND LOAD CARD C) BETWEEN BURN IN CARD AND DISPLAY/ OUTPUT MONITORING CARD.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>BILL OF MATERIALS, <strong>ONE WEEK BURN-IN TEST RESULTS</strong> (along with all Input/Output waveforms) &amp; FABRICATION FOLDER</td>
<td></td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>WARRANTY CERTIFICATE</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**APPENDIX –6**
APPENDIX – 7

WARRANTY CERTIFICATE

Name of the Vendor:

Name of the Indenter / subsystem:

Serial Number of the Jig:

Date of acceptance of Jig:

Warranty valid up to:

During warranty period, any defective parts or systems will be replaced free of cost.

(Vendor’s signature)

Note: - Warranty Certificate to be given by the vendor on vendor’s company letterhead.
### TABLE –1. MATERIAL REQUIREMENTS

<table>
<thead>
<tr>
<th>SL. NO</th>
<th>MATERIALS REQUIRED</th>
<th>FUNCTIONAL TEST JIG</th>
<th>BURN-IN JIG</th>
<th>REMARKS</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PCB</td>
<td>Glass Epoxy Laminate</td>
<td>Polymide Laminate</td>
<td>Burn-In board should withstand continuous operation of 125°C. PCB specifications are given separately.</td>
</tr>
<tr>
<td>2</td>
<td>Wires</td>
<td>PTFE (Teflon)</td>
<td>PTFE (Teflon)</td>
<td>Clear harness length should be minimum 2.2 meters for Burn-in jig. Wire Specifications are given separately.</td>
</tr>
<tr>
<td>3</td>
<td>Connector</td>
<td>FR022-grade</td>
<td>FR022-grade</td>
<td>Detailed connector specifications are given separately.</td>
</tr>
<tr>
<td>4</td>
<td>ZIF Socket</td>
<td>3M</td>
<td>3M</td>
<td>Part No. will be provided in Jig specifications</td>
</tr>
<tr>
<td></td>
<td>Socket</td>
<td>Azimuth</td>
<td>Azimuth</td>
<td>Part No. will be provided in Jig specifications</td>
</tr>
<tr>
<td></td>
<td>Socket</td>
<td>Yamaichi</td>
<td>Yamaichi</td>
<td>It’s lid is to be milled to place RCNW without damage</td>
</tr>
<tr>
<td>5</td>
<td>Electronic Components</td>
<td>Industrial-grade</td>
<td>Mil-grade</td>
<td>Correct value &amp; tolerance shall be used. Refer Appendix - 12</td>
</tr>
<tr>
<td>6</td>
<td>Sleeve</td>
<td>Shrinkable</td>
<td>Shrinkable</td>
<td>Recham Brand</td>
</tr>
<tr>
<td>7</td>
<td>Lacing Thread</td>
<td>Wax coated</td>
<td>Wax coated</td>
<td>Alpha Brand</td>
</tr>
<tr>
<td>8</td>
<td>Conformal coating</td>
<td>--</td>
<td>Polyurethane</td>
<td>Vendor need to get the material.</td>
</tr>
<tr>
<td>9</td>
<td>Solder Lead</td>
<td>5 core, SN63PB37</td>
<td>5 core, SN63PB37</td>
<td>Use 21 gauge RMA flux, with solder. <strong>Flux shall not be used while doing soldering on Burn-In board.</strong></td>
</tr>
</tbody>
</table>

### TABLE– 2 MECHANICAL SPECIFICATIONS.

<table>
<thead>
<tr>
<th>SL. NO.</th>
<th>NAME OF MATERIAL</th>
<th>SPECIFICATIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Sheet Metal</td>
<td>Thickness 1.2 to 1.5mm including powder coating. Box to be Powder coated</td>
</tr>
<tr>
<td>2</td>
<td>Mechanical Design of the box</td>
<td>CAD package to be used</td>
</tr>
</tbody>
</table>
3. Screws and Bolts | Stainless Steel  
4. Marking | Screen printable  
5. Size of the Box | Given in Appendix-9  
6. Color of the Box | Grey/Blue  

Burn-in board Size: Maximum 1’ X 1’

**TABLE 3 PROCUREMENT SPECIFICATIONS**

<table>
<thead>
<tr>
<th>SL. NO.</th>
<th>NAME OF MATERIAL</th>
<th>SPECIFICATIONS</th>
</tr>
</thead>
</table>
| 1       | PCB              | Gloss Epoxy Laminate  
FR4/ 135° C T9  
C1/C1; size – 18” X 24”  
IPC 4101 complaint, 62 mil thickness  
**Vendors: Micropack, Bangalore.**  
Polymide Laminate –  
Details are given in Appendix-8. |
| 2       | Wires            | PTFE (Teflon) – 24/EE  
Wherever the requirement changes, the gauge is to be specified in the indent.  
*For Communication Jigs, shielded cable shall be used in consultation with Subsystem, wherever required.*  
Details are given in Appendix-8. |
| 3       | Connectors       | Details are given in Appendix-8. |
| 4       | ZIF Socket       | 3M brand  
Details are given in Appendix-8.  
Yamaichi socket  
Part No: IC51-0444-400 |
| 5       | Electronic Components | Mil- grade; Value & tolerance shall be correct. The brand names are given in Table-8. |
| 6       | Sleeve           | Shrinkable sleeve from RECHAM |
| 7       | Lacing Thread    | Wax coated lacing thread from ALPHA |
| 8       | Solder Lead      | 5 core, SN63PB37 with 21 gauge RMA flux. |
SPECIFICATIONS OF CRITICAL PARTS AND MATERIALS

1. ZIF SOCKETS

MAKE: 3M
Distributor: M/s Pouyet Communication India Pvt Ltd,
138 Residency Road, Raheja Paramount
Bangalore-560 025.

<table>
<thead>
<tr>
<th>Size of ZIF socket</th>
<th>No. of pins</th>
<th>3M Part No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 &quot;X 1/2&quot;</td>
<td>24</td>
<td>224A–6313-OUA-1902</td>
</tr>
<tr>
<td>1 &quot;X 1/2&quot;</td>
<td>24</td>
<td>224A–6313-OUA-1902</td>
</tr>
<tr>
<td>1 &quot;X 1&quot;</td>
<td>24</td>
<td>224A–6313-OUA-1902</td>
</tr>
<tr>
<td>1 &quot;X 11/2&quot;</td>
<td>24</td>
<td>224A–6313-OUA-1902</td>
</tr>
<tr>
<td>1 &quot;X 11/2&quot;</td>
<td>24</td>
<td>224A–6313-OUA-1902</td>
</tr>
</tbody>
</table>

B. Yamaichi socket for 44 pin Jlead RCNW part no: Part No: IC51-0444-400
Note: It’s lid is to be milled to place RCNW without damage

2. POLYAMIDE BOARD

1) Manufacturer: MICRO PACK,
  Plot.No.16, Jigani Industrial Area
  Bangalore-562106

2) Material: NELCO make N 7000 –1

3) Board Size: 300mmx300mm

4) Type: DSB with PTH

5) Copper thickness: 70 microns

3. CONNECTORS

1) Make: Amphenol
Distributors: Amphenol Interconnect India Pvt Ltd
(Formerly Amphetronix Pvt Ltd)
4931 High point IV, 45 Palace Road
Bangalore-560001
## Connector Part Numbers – Amphenol

<table>
<thead>
<tr>
<th>Sl No</th>
<th>Type</th>
<th>Description</th>
<th>Part number</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Standard Density Crimpable Connectors</td>
<td>9-pin plug</td>
<td>4110-2-1-9P-GNMB-GND</td>
</tr>
<tr>
<td>2</td>
<td></td>
<td>15-pin plug</td>
<td>4110-2-1-15P-GNMB-GND</td>
</tr>
<tr>
<td>3</td>
<td></td>
<td>25-pin plug</td>
<td>4110-2-1-25P-GNMB-GND</td>
</tr>
<tr>
<td>4</td>
<td></td>
<td>37-pin plug</td>
<td>4110-2-1-37P-GNMB-GND</td>
</tr>
<tr>
<td>5</td>
<td></td>
<td>50-pin plug</td>
<td>4110-2-1-50P-GNMB-GND</td>
</tr>
<tr>
<td>6</td>
<td></td>
<td>9-pin socket</td>
<td>4110-2-1-9S-GNMB-GND</td>
</tr>
<tr>
<td>7</td>
<td></td>
<td>15-pin socket</td>
<td>4110-2-1-15S-GNMB-GND</td>
</tr>
<tr>
<td>8</td>
<td></td>
<td>25-pin socket</td>
<td>4110-2-1-25S-GNMB-GND</td>
</tr>
<tr>
<td>9</td>
<td></td>
<td>37-pin socket</td>
<td>4110-2-1-37S-GNMB-GND</td>
</tr>
<tr>
<td>10</td>
<td></td>
<td>50-pin socket</td>
<td>4110-2-1-50S-GNMB-GND</td>
</tr>
<tr>
<td>11</td>
<td>High density crimpable connector</td>
<td>78-pin plug</td>
<td>4110-2-2-78P-GNMB-GND</td>
</tr>
<tr>
<td>12</td>
<td></td>
<td>78-pin socket</td>
<td>4110-2-2-78S-GNMB-GND</td>
</tr>
<tr>
<td>13</td>
<td>Standard density contacts</td>
<td>Pin contact</td>
<td>4110-5-1-P-GNMB-GND</td>
</tr>
<tr>
<td>14</td>
<td></td>
<td>Socket contact</td>
<td>4110-5-1-S-GNMB-GND</td>
</tr>
<tr>
<td>15</td>
<td>High density contacts</td>
<td>Pin contact</td>
<td>4110-5-2-P-GNMB-GND</td>
</tr>
<tr>
<td>16</td>
<td></td>
<td>Socket contact</td>
<td>4110-5-2-S-GNMB-GND</td>
</tr>
<tr>
<td>17</td>
<td>Standard Density 90 degree bent PCB mountable Connectors</td>
<td>9-pin plug</td>
<td>4110-1-1-9P-4-GNMB-GND</td>
</tr>
<tr>
<td>18</td>
<td></td>
<td>15-pin plug</td>
<td>4110-1-1-15P-4-GNMB-GND</td>
</tr>
<tr>
<td>19</td>
<td></td>
<td>25-pin plug</td>
<td>4110-1-1-25P-4-GNMB-GND</td>
</tr>
<tr>
<td>20</td>
<td></td>
<td>37-pin plug</td>
<td>4110-1-1-37P-4-GNMB-GND</td>
</tr>
<tr>
<td>21</td>
<td></td>
<td>50-pin plug</td>
<td>4110-1-1-50P-4-GNMB-GND</td>
</tr>
<tr>
<td>22</td>
<td></td>
<td>9-pin socket</td>
<td>4110-1-1-9S-4-GNMB-GND</td>
</tr>
<tr>
<td>23</td>
<td></td>
<td>15-pin socket</td>
<td>4110-1-1-15S-4-GNMB-GND</td>
</tr>
<tr>
<td>24</td>
<td></td>
<td>25-pin socket</td>
<td>4110-1-1-25S-4-GNMB-GND</td>
</tr>
<tr>
<td>25</td>
<td></td>
<td>37-pin socket</td>
<td>4110-1-1-37S-4-GNMB-GND</td>
</tr>
<tr>
<td>26</td>
<td></td>
<td>50-pin socket</td>
<td>4110-1-1-50S-4-GNMB-GND</td>
</tr>
<tr>
<td>27</td>
<td>High Density 90 degree bent PCB Mountable Connectors</td>
<td>78-pin plug</td>
<td>4110-5-2-78P-GNMB-GND</td>
</tr>
<tr>
<td></td>
<td></td>
<td>78-pin socket</td>
<td>4110-5-2-78S-GNMB-GND</td>
</tr>
</tbody>
</table>

### 4. SHIELDED CABLES:

Manufacturer’s Address: Sanghvi Aerospace (p) Ltd.,
B/h Lalit Warehouse, Narol-Sarkhej Highway,
Narol, Ahmedabad – 382405, India

<table>
<thead>
<tr>
<th>Mil Part No.</th>
<th>Sanghvi Part No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hybrid cable single core (M27500 26WC1S24)</td>
<td>75981A-26-1S24</td>
</tr>
</tbody>
</table>
APPENDIX – 9

Mechanical BOX details of FTJ and BIJ

Shape of Box: -

1) Rectangular Box (only 2-piece design) with following dimensions:

From 12”(l) x 6”(w) x 6”(h) to 15”(l) x 9”(w) x 6”(h)

or

From 12” (l) x 9”(w) x 4”(h) to 15”(l) x 15”(w) x 9”(h)

Weight of Box: - Not more than 5kgs.

Thickness of the sheet metal (including coating) should be 1.2 mm to 1.5 mm.
### BILL OF MATERIALS – FTJ

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>Component Type</th>
<th>Component ID</th>
<th>Quantity</th>
<th>Quality Level</th>
<th>Component Part No.</th>
<th>Value with voltage/ Wattage specification</th>
<th>Tolerance</th>
<th>Manufacturer</th>
</tr>
</thead>
<tbody>
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</tbody>
</table>

Prepared By: (Vendor)

Approved by: (Subsystem, URSC)

Table -4
# BILL OF MATERIALS – BURN IN UNIT

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>Component Type</th>
<th>Component ID</th>
<th>Quantity</th>
<th>Quality Level</th>
<th>Component Part No.</th>
<th>Value with voltage/ Wattage specification</th>
<th>Tolerance</th>
<th>Manufacturer</th>
</tr>
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</tbody>
</table>

Prepared By: (Vendor)  

Approved by: (Subsystem, URSC)

Table -5
## BILL OF MATERIALS – BURN IN BOARD

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>Component Type</th>
<th>Component ID</th>
<th>Quantity</th>
<th>Quality Level</th>
<th>Component Part No.</th>
<th>Value with voltage/ Wattage specification</th>
<th>Tolerance</th>
<th>Manufacturer</th>
</tr>
</thead>
</table>

Prepared By: (Vendor)  
Approved by: (Subsystem, URSC)  

Table -6
### Measured Values of Components with Voltage/Wattage Ratings

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>Component ID</th>
<th>Measured Value</th>
<th>Voltage/Wattage rating</th>
<th>Remarks (Tolerance details etc.)</th>
</tr>
</thead>
<tbody>
<tr>
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</tr>
</tbody>
</table>

Prepared By: (Vendor)  
Reviewed By: (QC Inspector)  
Approved by: (Subsystem, URSC)
FUNCTIONAL TEST JIG APPROVAL FORMAT

1. Serial Number of FTJ:

2. Deliverables:
   a) Jig
   b) Document
   c) QC Inspection Report
   d) Approved Bill of Materials (as per the format given by HQCS)
   e) Warranty Certificate
   f) i) Approved PCB layouts of all PCBs, Spool files, Component Marking, PTH marking, Drilling details prints
      ii) Approved PCB film
      iii) Unit Interconnection Details
   The details mentioned in (f) above shall be submitted in hard copy in and soft copy in DVD form.
   g) Fabrication Folder & One HMC/RCNW test results

3. Electrical Functionality: Functioning in all respects: Yes/ No

Approved by: -
Subsystem Engineer with Date:
HQCS Engineer with Date:
BURN-IN JIG APPROVAL FORMAT

1. Serial Number of Burn-In Unit
   Serial Number of Burn-In Boards

2. Deliverables:
   a. Jig (Burn-In unit, Burn-In boards, Harnesses – specify no.of boards and harnesses)
   b. Document
   c. QC Inspection Report
   d. Approved Bill of Materials (as per the format given by HQCS)
   e. Warranty Certificate
   f. i) Approved PCB layouts of all PCBs, Spool files, Component Marking, PTH marking, Drilling details prints
      ii) Approved PCB film
      iii) Burn-In Jig interconnection details (as per the format given in SOW document)
      The details mentioned in (f) above shall be submitted in hard copy and soft copy in DVD form.
   g) Fabrication Folder &One week burn-in test results with waveforms.

4. Electrical Functionality: Functioning in all respects: Yes/ No

5. Conformal Coating done: Yes/ No

Accepted By: -
   Subsystem Engineer with Date:
   HQCS Engineer with Date:

APPENDIX-11
### APPENDIX –12

<table>
<thead>
<tr>
<th>Component type</th>
<th>Quality level</th>
<th>Manufacturer</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resistor</td>
<td>Industrial</td>
<td>Watts, Keltron</td>
</tr>
<tr>
<td>Resistor</td>
<td>Mil grade</td>
<td></td>
</tr>
<tr>
<td>Capacitor</td>
<td>Industrial</td>
<td>Philips, Keltron</td>
</tr>
<tr>
<td>Capacitor</td>
<td>Mil grade</td>
<td>Vishay</td>
</tr>
<tr>
<td>IC</td>
<td>Industrial</td>
<td>Philips/NS, FAIRCHILD</td>
</tr>
<tr>
<td>IC</td>
<td>Mil grade</td>
<td></td>
</tr>
<tr>
<td>ZIF</td>
<td></td>
<td>3M</td>
</tr>
<tr>
<td>LED</td>
<td>Industrial</td>
<td>Watts, Liton</td>
</tr>
<tr>
<td>Banana Socket</td>
<td>Industrial</td>
<td>Elcom</td>
</tr>
<tr>
<td>PB Socket</td>
<td>Industrial</td>
<td>Elcom</td>
</tr>
<tr>
<td>Switch</td>
<td>Industrial</td>
<td>Elcom</td>
</tr>
<tr>
<td>Wires</td>
<td>Industrial- Teflon</td>
<td>Tanya Enterprises-Meerut</td>
</tr>
<tr>
<td>Shielded Cable</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Connectors</td>
<td></td>
<td>Amphenol</td>
</tr>
<tr>
<td>Toggle Switch</td>
<td>Industrial</td>
<td>Elcom</td>
</tr>
<tr>
<td>Terminal posts</td>
<td>Industrial</td>
<td>Elcom</td>
</tr>
<tr>
<td>Sockets</td>
<td>Industrial</td>
<td>Elcom</td>
</tr>
<tr>
<td>Binding post</td>
<td>Industrial</td>
<td>Elcom</td>
</tr>
<tr>
<td>Binding post</td>
<td>Mil grade</td>
<td></td>
</tr>
</tbody>
</table>